

Sinclair

Spectrum 128

Service Manual

USE SPECTRUM CIRCUITS.

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SERVICING MANUAL
FOR
SPECTRUM 128 ©

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SECTION 1

SYSTEM DESCRIPTION

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1. INTRODUCTION

- 1.1 The Spectrum 128 is a derivative of the 48K Spectrum Plus offering 128K of RAM, music quality **sound**, greatly improved video quality and higher hardware reliability.
- 1.2 The firmware is **capable** of running in Spectrum **48K** mode or, **alternatively** in 128K mode, which **will** support paged memory in the **form** of a RAM disk. Extended BASIC to handle the sound facility is provided, and a full screen editor is incorporated in the firmware.

1.3 A **list** of the **principle** features appears below:

- (a) 128K dynamic RAM
- (b) 32K ROM
- (c) Numeric keypad
- (d) TV sound with composite video
- (e) Elimination of dot crawl (single crystal operation)
- (f) RGB output
- (g) RS232 serial port
- (h) Musical instrument digital interface (MIDI)
- (j) Software compatible with all previous **Spectrums**
- (k) Edge connector **compatible** with Spectrum.

2. ARCHITECTURE

2.1 The architecture of the Spectrum 128 shown in Figure 1.1 is **typical** of many microcomputer systems is that it comprises a single **microprocessor** chip (in this instance a Z80A or u780), a read only memory (ROM) a paged random access memory (RAM) and an input-output section. The latter **handles** the keyboard input, tape and TV display functions using the logic gate array (ULA **IC1**), and the keypad input, sound and RS232/MIDI interfaces using the sound generator circuit IC32.

2.2 The analogue **circuits** (not shown) generate the 17.7 MHz master **clock**, and process the RGB colour monitor and sound signals. The resultant outputs are suitable for use with colour (RGB) or black and white monitors, and domestic UHF television receivers. A modulated sound carrier is output with the composite video.

2.3 The computer is built on a single printed **circuit** board which **also** includes a **regulated** power supply fed from an external 9V power pack. The keyboard matrix is part of the upper case assembly and is connected to the board via two ribbon cables KB1 and K82. A digital keypad is **also** provided, connected via a flexible cable. It can be used as a games controller or calculator pad and has special function keys for use with the full screen editor. An in-built peripheral interface controller (PIC) performs the keypad scanning routines and delivers an output to the Z80 on demand.

3. Z80A CPU

3.1 The Z80A is an 8-bit **single** chip central processing unit (CPU). It is **clocked** at 3.5 MHz from a divide of an external source **controlled** by the logic gate array (ULA) and has a standard three bus input/output arrangement. These buses are the data Bus, Address Bus and Control Bus **respectively**.

- 3.2 Data Bus. **D7-D0** constitutes an 8-bit bi-directional data bus with active high, tri-state **input/outputs**. It is used for data exchanges with the memory, sound chip and the ULA.
- 3.3 Address Bus. A15-A0 constitutes a 16-bit address bus with active high, tri-state outputs. The address bus provides the address for memory data exchanges and for data exchanges with the ULA. It is also used during the interrupt routine (see below) when scanning the keyboard matrix.
- 3.4 **Control** Bus. The control bus is a collection of individual signals which generally organise the **flow** of data on the address and data buses. The block diagram only shows five of these **signals although** others of minor importance are made **available** at the expansion port (see Figure 1.5 for details).
- 3.5 Starting with memory request (**MREQ**), this signal is active low indicating when the address bus holds a valid address for a memory read or memory write operation. Input/Output request (**IORQ**) is also active low but indicates when the address bus holds a valid address for I/O read/write operations.
- 3.6 The read and write signals (**RD** and **\overline{WR}**) are active **low**, and one or other is active indicating that the CPU wants to read or write data to a memory location or I/O device. All the control **signals** discussed so far are active low, tri-state outputs.
- 3.7 The last **control** signal described here is the maskable interrupt (**INT**). This input is active low and is generated by the ULA once every 20 **ms**. Each time it is **received** the CPU **'calls'** the **'maskable interrupt'** routine during which the real-time clock is incremented and the keyboard and keypad **scanned**.
- 3.8 CPU Clock. Returning to the CPU clock mentioned earlier in this section, the ULA is able to inhibit this input bringing the CPU to a temporary **halt**. This mechanism gives the ULA absolute priority, allowing it to access the contended RAM without interference from the CPU (see RAM description). Switching transistor TR3 ensures that the clock amplitude is +5V rather than some arbitrary TTL level. This is essential if the CPU is to operate effectively **while** executing fast machine code programs of the **'space invader'** type.
- 3.9 Dynamic Memory Refresh. The CPU incorporates **built-in** dynamic RAM refresh circuitry. As part of the instruction OP code fetch cycle, the CPU performs a memory request after first placing the refresh address on the lower eight bits of the address bus. At the end of the cycle the address is incremented so that over 255 fetch cycles, each row of the dynamic RAM is refreshed.

4.3 The Z80 address space is allocated according to the two **m.s.** bits of the address bus (**ZA14,15**) and the contents of the bank register IC31 which is at address **7FF0_H** in the **Z80's** I/O space. The significance of the register bits is summarised **below**:

Bits	Function
B2-B0	Selects the page occupying the top 16K of the Z80 address space. Any RAM page can occupy the space.
B3	Instructs the ULA to access the display mapped in page 5 or 7. Bit set : screen in page 7 Bit clear : screen in page 5
B4	Determines whether instruction fetches are from ROM 0 or ROM 1* Bit set : fetches from the 48K Spectrum ROM (ROM 1) Bit clear : fetches from the 128K Spectrum ROM (ROM 0)
85	Set to prevent further accesses to the bank register (protection against SPECTRUM programs crashing if the bank register is written to in error)

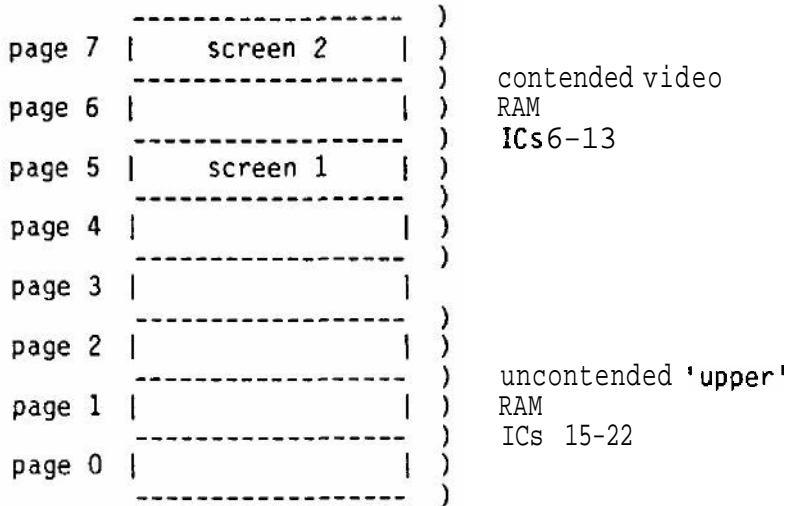
* see para. **4.12.2**

4.4 Clearly, dependent on register bits B2-B0, the Z80 can access page 2 at address **8000_H** or **C000_H** and the screen in page 5 at address **4000_H** or **C000_H**. The screen in page 7 can **only** be accessed at address **C000_H**. On power up, or after reset the bank register is **cleared** and loads page 0 at address **C000_H**, selects the 128K Spectrum ROM at address **0000_H** and informs the ULA that screen accesses are from page 5.

This **mechanism only** applies to the non-contended RAM area. An alternative refresh method is adopted for the contended RAM.

4. MEMORY ORGANISATION

4.1 The Spectrum 128 has 160K bytes of addressable memory - a 32K byte ROM (IC5) and 128K bytes of dynamic RAM (IC6-IC22). The latter is organised as eight 16K byte pages as indicated **below**.



4.2 Pages 0-3 are uncontended and are accessed solely by the Z80. Pages 4-7 are contended in that the Z80 and ULA IC1 both require access to pages 5 and 7 in order to generate the memory mapped **displays**. The address of any page of RAM depends on where it appears in the address space of the Z80 which is structured as **follows**:

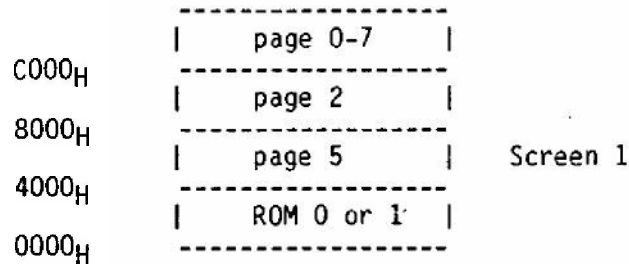


TABLE 5.1 CASE ASSEMBLY

DESCRIPTION	MANUFACTURE
Base Assembly	
Final PCB Assembly - Table 5.2	
Heatsink	
Retractable Legs - 2 off	
Leg Springs - 2 off	
Bottom Case Moulding	
Fixings	
1/4 in self tap screw - 3 off)	PCB
Fibre washer - 3 off)	
5/16 in self tap screw (2 off) -	heatsink
M3 x 10mm pan hd screw - 1 off)	
M3 plain washer - 1 off)	voltage
M3 crinkle washer - 1 off)	regulator
M3 hex nut - 1 off }	
1 Keyboard Assembly	
I Keyboard Reaction Plate	
Spectrum + Membrane	
Bubble Mat	
Upper Case Moulding	
Key Set	
Tail Clamps - 2 off	
Fixings	
Double sided adhesive tape	
12mm wide (Tesafix 959) -	tails
1/4 in self tap screw (4 off) -	tail
	clamps
5/16 in self tap screw (10 off) -	reaction
	plate
General Assembly Fixings	
5/16 in self tap screw - 6 off)	base/
1/2 in self tap screw - 2 off)	keyboard

SECTION 5

PARTS LIST

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1. INTRODUCTION

1.1 Parts lists for the SPECTRUM 128 are provided in table form; one for the case **assembly** (Table 5.1), one for the main pcb assembly (Table 5.2) and another for the keypad pcb assembly (Table 5.3). PCB layout diagrams are given in Figures 5.1 and 5.2 ;the notes to be found in **Table 5.2** are explained below.

2. NOTES TO TABLE 5.2

- (1) All RAM chips should have 150ns access time and 128 row refresh. This includes parts from the following manufacturers: Hitachi, **Intel**, **Mitsubishi**, Mostek, Motorola, NEC, OKI, Panasonic, Toshiba and National.
- (2) If TR3 is type KSC839, resistor R24 should be 15K0.
- (3) Provision has been made on the pcb for a 2 to 22pF film dielectric trimmer should the need arise.
- (4) The ROM should be pin compatible with a 27256 EPROM and have an address **access** time of less than 400 ns. The output enable access time **should** be less than 250 ns.
- (5) The **crystal** is series resonant with 20pF and accurate to 10 ppm absolute, + 10 ppm 20 to 60°C, ± 5 ppm per year.
- (6) If preferred, the 20uF capacitor used for C124 may be split into two parallel capacitors of 10 pF ± 2% in the positions C124 and C130.
- (7) For FTZ (German) version only.
- (8) 6.0 MHz version (Type No ? } for use in the UK; 5.5 MHz version (Type No ?) for use in most other European countries.

4.5 All memory accesses are **controlled** by the programmable **logic** array (PAL) IC29. It does this by decoding the two m.s. Z80 address bits **Z15**, Z14 with bits B2-B0 from the bank register to produce three pairs of supplementary address lines. They are:

- (a) **UA15,14** specifying the page number in the uncontended RAM space
- (b) **VA15,14** specifying the page number in the contended RAM space
- (c) **ULA15,14** controlling bus arbitration and Z8Q access to the ROM and contended RAM space.

4.6 The decodes are summarised **below** and described in the **following paragraphs**.

Z80 operation	ZA15	ZA14	B2	B1	B0	ULA15	ULA14	VA15	VA14	UA15	UAH
R O M access	0	0	X	X	X	0	0	X	X	X	X
4000 _H -7FFF _H	0	1	X	X	X	0		1	0	1	X
8000 _H -8FFF _H	1	0	X	X	X	1	0	X	X	1	0
page 0 access	1	1	0	0	0	1	X	X	X	0	0
page 1 access	1	1	0	0	1	1	X	X	X	0	1
page 2 access	1	1	0	1	0	1	X	X	X	1	0
page 3 access	1	1	0	1	1	1	X	X	X	1	1
page 4 access	1	1	1	0	0	0	1	0	0	X	X
page 5 access		1	1	0	1	0	1	0	1	X	X
page 6 access	1	1	1	1	0	0	1	1	0	X	X
page 7 access	1	1	1	1	1	0	1	1	1	X	X

4.7 ZA15 = ZA14 = 0. These bits select the first 16K of Z80 address space beginning at 0000_H, and result in the PAL generating ULA15 = ULA14 = 0. These are decoded by the ULA (IC1) to produce a signal ROMCS enabling the ROM IC5. A13-A0 on the Z80 address bus provide the instruction address, bank register bit 4 determines whether the upper or lower 16K of ROM is accessed.

4.8 ZA15 = 0, ZA14 = 1. These bits select the RAM page located in the second 16K of the Z80 address space beginning at 4000_H and result in the PAL generating ULA15 = VA15 = 0 and ULA14 = VA14 = 1. The ULA lines signal an access of the contended RAM area and prompt IC1 to assert the DRAS, CAS and DRAMWE lines **controlling** the read/write operation. At the same time, ULA15 inhibits the CAS output from IC27 preventing any access to the uncontended RAM area.

4.9 The 2:1 data **selector** IC30 supplies the m.s. row and column address bits to the contended RAM as DMA7, first **selecting** the row address VA14 = 1 while DRAS is low and the column address bit VA15 = 0 when it returns high. This combination **selects** the second 16K bank of RAM in the contended area, allowing DMA6 - DMA0 to access locations in page 5 used for the standard screen display.

- 4.10 ZA15 = 1, **ZA14** = 0. These **bits** select the RAM page appearing in the third 16K of the Z80 address space beginning at **8000H**, and result in the PAL generating ULA15 = **UA15** = 1 and ULA14 = **UA14** = 0. The ULA lines signal an access to the uncontended RAM area and **enable** IC27 to assert the CAS line which together with RAS (**MREQ**) and **WR control** the read/write operation. (Access control lines for the contended RAM area generated by IC1 i.e. **CAS**, DRAS and **DRAMWE**, are not asserted at this time). VA15 and VA14 **respectively supply** the **m.s.** row and column address bits for the uncontended RAM area as MA7 and **select** the second 16K bank of RAM allowing MA6-MA0 to access locations in page 2. .
- 4.11 ZA15 = ZA14 = 1. These bits **select** the RAM page appearing in the top 16K of the Z80 address space beginning at **C000H**. The bits together with B2-B0 from the bank register IC31 are decoded by the PAL to select any page from the RAM according to the setting of the supplementary address line pairs. For the uncontended RAM space ULA15 is **always** high allowing IC27 to control read/write operations. **UA15,14** assume one of four possible states reflecting the state of **B1,B0** and select a page in the range 0-3. For contended RAM accesses ULA15 is always low allowing IC1 to control the read/write operations, and the data selector **IC30** to deliver the m.s row and column address bits **VA14,15**. The latter also assume one of four states and since B2 is set, **selects** a page in the range 4-7.
- 4.12 Read/Write Operations and Bus Arbitration
- 4.12.1 The following description should be read in conjunction with the circuit diagram given in **Figure 1.5**
- 4.12.2 Read **Only** Memory (**IC5**). The **physical** ROM is a 32K byte device, but appears in the Z80 address space as two separate 16K ROM's. ROM 1 is the old **48K** Spectrum ROM (**slightly** modified) and is selected when bank register bit 4 sets address A14. ROM 0 is the new Spectrum 128 ROM and is selected when bit 4 is **clear**. **CPU** accesses occur during memory read **cycles** when the Z80 asserts **MREQ** and loads the address bus A13-A0. **MREQ** enables the ROM outputs onto the data bus D7-D0, ROMCS decoded from **ZA14,15** (see para. 4.7) **selects** the **chip**.
- 4.12.3 An external ROM chip select input, supplied via the expansion port on pin 25A, selectively **disables** the **on-board** ROM by pulling the select input high. By virtue of R33 placed on the ULA side of the ROM the ULA ROMCS output is effectively inhibited. Interface 1 uses this mechanism, allowing the CPU to read the extension ROM in the interface for **microdrive** and RS232 **applications**.

- 4.12.4 **Uncontended RAM (IC15-22).** The **uncontended** RAM comprises eight 64K dynamic RAM chips organised as a 64K byte memory with a 256 x 256 row/column matrix. When **ULA15** is high (see para. 4.11) separate 8 bit row/column addresses are supplied by IC27 as **MA7-MA0**. These are derived from the Z80 address bus A13-A0 with **UA14** and **UA15** from IC29. The low order address bits **A6-A0** with **UA14** provide the row address and are **selected** at the beginning of the memory access cycle when **initially** the $\overline{\text{RAS}}$ (**MREQ**) output from **the Z80** is low. Later, as the row address is **latched**, IC27 asserts $\overline{\text{CAS}}$ **selecting** the high order address bits **A13-A7** with **UA15**.
- 4.12.5 Row/column address selection and RAS/CAS timing for the RAM is decoded in IC27 in conjunction with IC28 and the associated **discrete** components. A **theoretical** timing diagram illustrating the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ waveforms is given in Figure 1.2 (A read operation is shown when the **WRL** line from the Z80 is high).
- 4.12.6 Contended RAM (IC6-13). The organisation of the contended and uncontended RAM described above is **identical**. However, because **ULA15** is low during accesses to the contended area, **IC27 only** sources a 7-bit row/column address **DMA6-DMA7**. The **m.s** address bit is sourced by the 2:1 data selector IC30. At the start of the memory access cycle **Id** asserts **DRAS** and selects the row address as A13-A7 off the Z80 address bus with **VA14** via the selector. Later as the row address is latched **Id** sets **DRAS** and selects the column address as A6-A0 with **VA15**.
- 4.12.7 **RAS/CAS timing** for the contended RAM area is decoded by the ULA **IC1** from **MREQ** and **A15**. $\overline{\text{OCAS}}$ is asserted a short time after **DRAS** returns high, and latches the column address. **ULA15** prevents **IC27** generating an identical signal for the uncontended **RAM**. The **DRAMWE** signal, also generated by the ULA, is a decode of the $\overline{\text{RD}}$ / $\overline{\text{WR}}$ waveforms and selects a RAM read or RAM write cycle.
- 4.12.8 It **will** be apparent from the circuit diagram that the ULA can access the contended RAM by generating a set of addresses independent of those generated by the CPU. The address port for the RAM is therefore **dualled** by the insertion of small value series resistors on the address lines between IC27 and the RAM. This ensures that where there is likely to be **conflict** between the ULA and CPU, the ULA address has priority. Priority is assigned on the basis that the ULA must access screen pages 5 and 7 at set intervals in order to **build** up the video for the TV display. If the ULA is about to access the RAM and it detects either **A14** or **A15** (i.e the CPU is **also** about to access the RAM) the ULA inhibits the CPU clock temporarily halting the CPU memory transaction until its own transaction is completed.

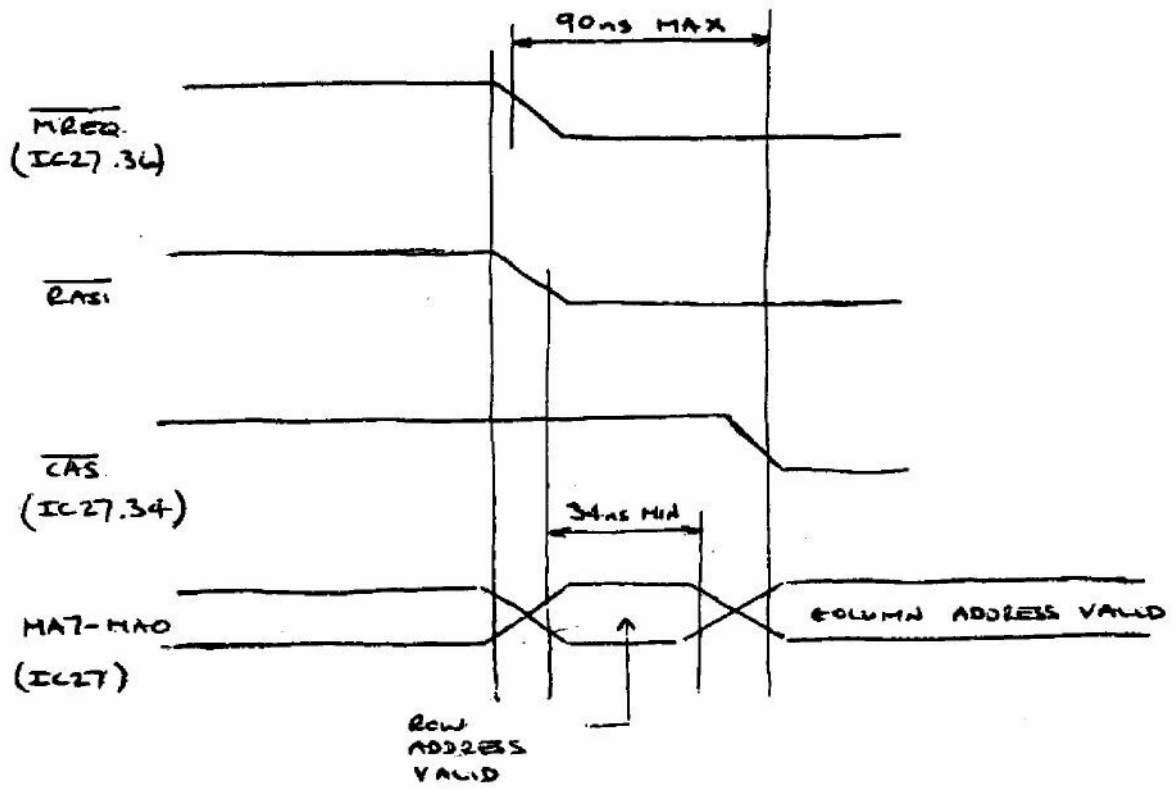


FIGURE 1.2 UNCONTENTED RAM $\overline{RAS}/\overline{CAS}$ TIMING (READ CYCLE SHOWN)

1.10

- 4.12.9 Resistors **R1** to **R8**, in series with the data bus lines, perform a similar function to the address port resistors **described** above. They ensure that the **ULA** does not '**see**' CPU write data while the **ULA** is accessing the contended RAM.
- 4.12.10 Refresh for the contended RAM is accomplished during normal read cycles, i.e. most rows are refreshed each time the **ULA** accesses screen pages during picture compilation; the remaining rows are refreshed as a result of other read cycles also known to occur at regular intervals within the refresh period.
- 4.12.11 Bank Register (IC31). The bank register is at address **7FFD_H** in the Z80 address space. The register is positive edge triggered and latches **D5-D0** off the data bus on the negative (trailing) edge of the **BANK** output from the PAL IC29. **BANK** is decoded (set high) from **IORQ** and **RD/W_R** active low (I/O read or write cycle) and **ZA1** and **ZA15** low (address **7FFD_H**).
- 4.12.12 On selecting the 48K Spectrum mode, the Z80 writes a '**1**' into bit 5 of the register, thus preventing any further access. This action preserves the Z80 address space, preventing erroneous calls to address **7FFD_H** crashing the SPECTRUM program. The bit can only be cleared by using the RESET pushbutton or by interrupting the power supply input.

5. INPUT/OUTPUT

- 5.1 The input/output functions are controlled by the Z80 in conjunction with the **ULA (IC1)** and the sound generator circuit **IC32**. Like its counterpart in the 48K Spectrum, the **ULA** handles the tape recorder read/write functions, and generates an interrupt during which it scans the main keyboard. It also accesses the contended RAM area **while** generating the drive waveforms for the TV display and produces a simple tone output while obeying the BEEP instruction.
- 5.2 The sound generator produces high quality music sound by mixing the outputs from up to three programmable tone generators and a noise generator. It also **handles** the **RS232/MIDI** interface and reads the keypad status. Each of these functions and the supporting circuits is described below.
- 5.3 TV Picture Generation and Sound Output
 - 5.3.1 The video compilation section of the **ULA** operates in conjunction with the memory mapped picture display area in the contended RAM, together with the colour encoder IC36 and UHF modulator. This combination produces a high resolution 24 line x 32 character, eight colour display **suitable** for use with RGB colour or **black** and white monitors or a domestic TV receiver. The sound output from the **ULA** or the programmable sound generator is FM modulated and added to the composite video signal for playback through the TV loudspeaker. If a monitor is used the sound is available through the MIC socket.

5.3.2 From the 17.73 MHz external clock (X1/IC37) the ULA derives line and field timing for the composite sync **signal** on pin **23**, and a pixel clock for timing **accesses** to the RAM. The ULA also generates two 8.8 MHz clocks on pins 46, 47 from which the encoder derives the 4.43 MHz reference and quadrature chroma **sub-carriers**. The fact that the **pixel** and chroma carriers are **derived** from the same **external** clock source means that dot crawl is eliminated. The dot pattern itself is minimised by adjusting the **display** line length.

5.3.3 The digital RGB and bright-up signals available from the ULA on pins 19-22 are derived by accessing the picture information located in page 5 or 7 of the contended RAM area at the **pixel** rate (para. 4.12.8). The addresses are necessarily independent of the CPU and appear on the ULA **address lines DMA6** to DMA0 and DMA7 as two separate bytes, timed by the $\overline{\text{RAS}}/\overline{\text{CAS}}$ **row/column address select** lines. DMA7 is a decode of bit 3 (**VB**) loaded in the bank register IC31 and sets the m.s row/column address bits as **follows**:

VB (IC31)	DMA7 (ULA) ROW	DMA7 (ULA) COLUMN	RAM PAGE
0	1	0	5
1	1	1	7

5.3.4 The RGB colour, bright-up and composite sync **signals** (Figure 1.6) are coupled to the RGB output socket via 68 ohm resistors and are suitable for direct input to a wide range of colour monitors. The same signals are also applied to the encoder IC36 to produce a composite video output at pin 6. The video comprises the **following** components.

- a) Line/frame sync with **colour** burst, derived from the composite sync input CS and a burst **oscillator** sustained by tank circuit L3. The position of the burst relative to the line sync pulse is determined by a threshold **level** set-up on the RAMP input of IC36 by R113/C115.
- b) Colour chrominance is derived by modulating the chroma sub-carriers with the colour difference signals decoded from the RGB and bright-up signals. The latter are first combined using a diode matrix D20-D25 to produce six colour inputs for IC36 - two for each colour, designated '0' and '1'. Without bright-up the presence of any **digital** colour input at logic '1' drives the '1' input only, producing a pixel display with the **colour** intensity set for normal viewing. With bright-up activated the '0' and '1' inputs are driven, increasing the intensity so as to highlight the pixel **display**.

- c) Luminance (grey scale) derived by mixing the RGB inputs in a fixed proportion. The signal is used to produce the colour difference signals in (b) and in its own right to drive the black and white monitor. The luminance is brought out at IC36 pin 7 and is applied to the RGB output socket via a **complimentary** transistor pair **TR13,14**.

The luminance is returned to IC36 mixed **with** the **FM** modulated sound carrier from IC38. The sound modulator operates at 6 MHz in the UK (5.5 MHz in most other European countries) and is tuned by L4. The modulating signal is derived either by the ULA **sourced** via R112/C123 or the sound generator circuit IC32 via R132/C127.

- 5.3.5 The composite video signal at IC36 pin 6 is **finally** applied to an encapsulated **UHF** modulator operating on European standard channel 36. The device is current driven via **TR10,11,12** to give improved linearity thus reducing the effect of sound on vision and vice-versa. The effect is further reduced by outputting the sound carrier **20dB** down with respect to the picture carrier.

5.4 Keyboard Scanning

- 5.4.1 Every 20ms (**i.e.** once per **maskable** interrupt), the CPU systematically scans the keyboard recording which keys (if any) have been depressed. The scanning method is described below with the aid of Figures 1.3 and 1.4. As the figures **clearly** illustrate the main keyboard consists of an upper and lower membrane. The upper membrane is organised as an 8 x 5 matrix, the intersection of each row and column bridged by a normally open switch contact. The **lower** membrane is organised in a similar manner except that only 16 of the intersections are **populated** by switch contacts. The row **'outputs'** and column **'inputs'** are shown connected in both cases to separate ribbon cables **KB1** and **KB2**, one to the ULA and the other to the high order address lines A15-A8. Pull-up resistors R65 through R69 ensure that when the address bus is in the high Z state, or none of the switch contacts is closed, row outputs **KB1-KB4** remain **high**.
- 5.4.2 When the keyboard scanning routines are entered **the** CPU performs successive I/O read cycles setting the **IORQ** and **RD** lines to the ULA, low. At the same time, the I/O port addresses placed on the upper **half** of the address bus are modified with each cycle such that each of the address lines A15 through A8 is set low in **turn**, the other lines remaining high.
- 5.4.3 The sequence starts with I/O port address FE driving address line **A8 low**. The keyboard matrix also sees this potential on **column 6**, **applied** via D6 and the ribbon cable **KB2**. Thus, when any of the switches on the intersection with the column is **pressed**, the corresponding row output **supplying** the ULA via the second ribbon **cable** (**KB1**), is pulled low.

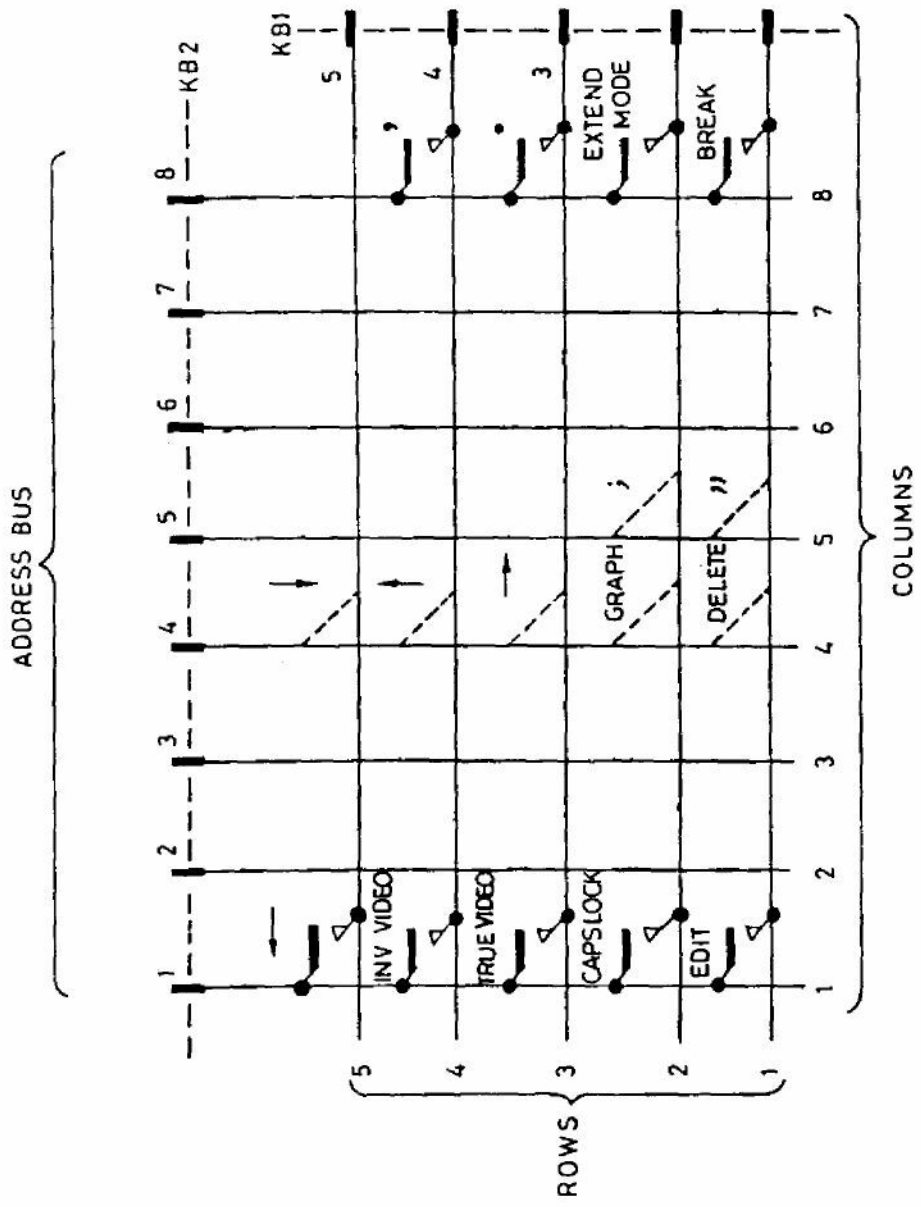


FIG 1.44 KEYBOARD LOWER MEMBRANE

5.4.4 The row **signal(s)** is **subsequently** buffered by the **ULA** and placed on one of the five low order data bus lines. For example, if the **CAPS SHIFT** key is pressed, row one output drives data bus **D0** high, and so on. The sequence ends **with** I/O address **7F** when column 8 is addressed. In this instance, operation of the **SPACE** key drives **D0** high. Clearly, the keyboard scanning routines make the distinction between the **CAPS SHIFT** and **SPACE** key by knowing which address line is being driven.

5.4.5 If one of the following keys is pressed the corresponding switch contact on the **lower** membrane is closed. **Additionally**, the **CAPS SHIFT** switch contact on the upper membrane closes.

TRUE VIDEO	EXTEND MODE	CURSOR →
INV VIDEO	EDIT	CURSOR ←
BREAK	CAPS LOCK	CURSOR ↑
DELETE		CURSOR ↓
GRAPH		

5.4.6 For example, pressing **TRUE VIDEO** closes the switch contact at row 1, column 6 on the upper membrane (**CAPS SHIFT**) and row 3, column 1 on the lower membrane (**TRUE VIDEO**).

5.4.7 Similarly, pressing any of the following keys results in the corresponding switch contact on the lower membrane closing as well as the **SYMBOL SHIFT** switch on the upper membrane:

, (comma)
 . (full-stop)
 ; (semi-colon)
 " (quotes)

5.4.7 For example, pressing full stop closes the switch contact at row 2, column 8 on the upper membrane (**SYMBOL SHIFT**) and row 3, column 8 on the lower membrane (**full stop**).

5.5 Tape Interface

5.5.1 When **LOADing** or **SAVEing** programs using a cassette recorder, the **ULA** transfers information between the **MIC** and **EAR** sockets and the data bus, performing **A/D** and **D/A** conversions as required. During the **LOAD** operation the CPU executes successive I/O read cycles to I/O port address 254, reading the **EAR** input off bus line **D6**. When performing a **SAVE** operation, the CPU executes successive I/O write cycles to I/O port address 254, this time writing data to the **MIC** output via bus line **D3**.

5.5.2 To ensure that I/O cycles are correctly implemented, the IORQ line supplying the ULA is gated with address line A0 via TR6. Thus, if any memory transactions occur when A0 is high (i.e. not port address 254) then the IORQ input is forced high inhibiting any attempt to perform the I/O cycle.

5.5.3 ULA Sound Output. It should be noted that while SAVEing, the level of the MIC output is barely sufficient to modulate the sound carrier to IC38. However, during the execution of a BEEP instruction the CPU writes instead to port 254 on bus line D4. This effectively boosts the MIC output, modulating the sound carrier so that the BEEP tone can be easily heard.

5.6 Programmable Sound Generator

5.6.1 The audio from the sound generator IC32 is derived from a master clock input supplied by the ULA, controlled and shaped in accordance with instruction codes loaded by the Z80 into 14 internal byte wide registers (see below).

REGISTER		BIT								
		B7	B6	B5	B4	B3	B2	B1	B0	
R0	Channel A Tone Period	8 BIT Fine Tune A								
R1						4 BIT Coarse Tune A				
R2	Channel B Tone Period	8 BIT Fine Tune B								
R3						4 BIT Coarse Tune B				
R4	Channel C Tone Period	8 BIT Fine Tune C								
R5						4 BIT Coarse Tune C				
R6	Noise Period						5-BIT Period Control			
R7	Enable	IN OUT*		Noise			Tone			
		IOB	IOA	C	B	A	C	B	A	
R10	Channel A Amplitude				M	L3	L2	L1	L0	
R11	Channel B Amplitude				M	L3	L2	L1	L0	
R12	Channel C Amplitude				M	L3	L2	L1	L0	
R13	Envelope Period	8 BIT Fine Tune E								
R14		8 BIT Coarse Tune								
R15	Envelope Shape/Cycle	CONT ATT ALT HOLD								
R16	I/O Port A Data Store	8 BIT PARALLEL I/O on Port A*								
R17	I/O Port B Data Store	8 BIT PARALLEL I/O on Port B								

* RS232/MIDI interface (see below)

5.6.2 The Z80 specifies a register by loading the data bus while writing to address $FFFD_H$ in the I/O space. DA3-DA0 supply the octal address between 0 and 15, DA7-DA4 should be all zero. (In the address mode, DA7-DA4 with IC32 pin 17 strapped high externally, are decoded in IC32 to provide a 'chip select' signal). The instruction code is then written to the register by writing to address $BFFD_H$.

BC1 and BDIR, decoded in D26,27 from PSG, AH and RDL, define the type of write **operation** for the sound generator as follows:

PSG	A14	RD	BDIR	BC1	I/O ADDRESS	OPERATION
0	X	X	0	0	-	INACTIVE
1	1	1	1	1	FFFD _H	WRITE ADDRESS
1	0	1	1	0	BFFD _H	WRITE DATA
1	1	0	0	1	FFFD _H	READ DATA*

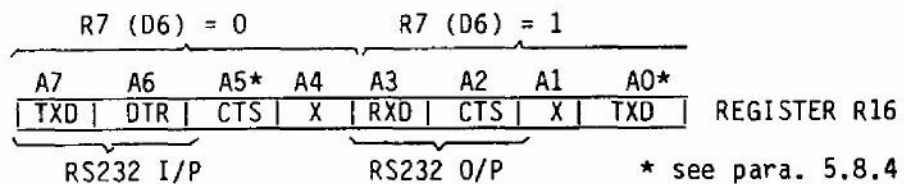
* RS232C/MIDI interface (see below)

5.6.3 PSG is decoded in IC29 from \overline{TORQ} with \overline{RD} or \overline{WR} (I/O read/write cycle) and ZA1 = 0 and ZA 15 = 1 (address FFFD_H with A14 high; address BFFD_H with A14 low).

5.7 RS232C/MIDI INTERFACE

5.7.1 The RS232C/MIDI interface is implemented using the Port A Data Store in the sound generator chip IC32. The data store is a special register at octal address 16 which accesses an 8-bit **bi-directional** port A7-A0. The port occupies the same I/O space as the sound generator registers and is accessed in much the same way. The addition of a read **cycle** at I/O address FFFD_H allows the Z80 to input data.

5.7.2 The port direction is determined by a control bit written to register R7 on bus line D6. When D6 is low the port is configured as an input and when high as an output. In this **application** A3-A0 are only used as outputs and A7-A4 as inputs. A3/A2 supply an RS232C driver IC33 which converts the TTL outputs to RS232C levels (+12V); A2 and A3 drive the CTS and RXD interface lines **respectively**. A4 - A7 are supplied from an RS232C receiver IC34 which converts the RS232C inputs to TTL levels; A6 and A7 are driven by the DTR and TXD interface lines **respectively**. The data register contents are summarised as follows:



5.7.3 It is evident from the **signal** directions that the Spectrum 128 adopts the **role** of a data communications equipment (DCE). However, DTR and CTS do not perform a handshake but are the same signal transmitted in opposite directions. The transmission format is **asynchronous, full** duplex with 11-bit data frames comprising 1 start bit, eight data bits and two stop bits. Two stop bits are always sent, but the interface can receive **satisfactorily** with one

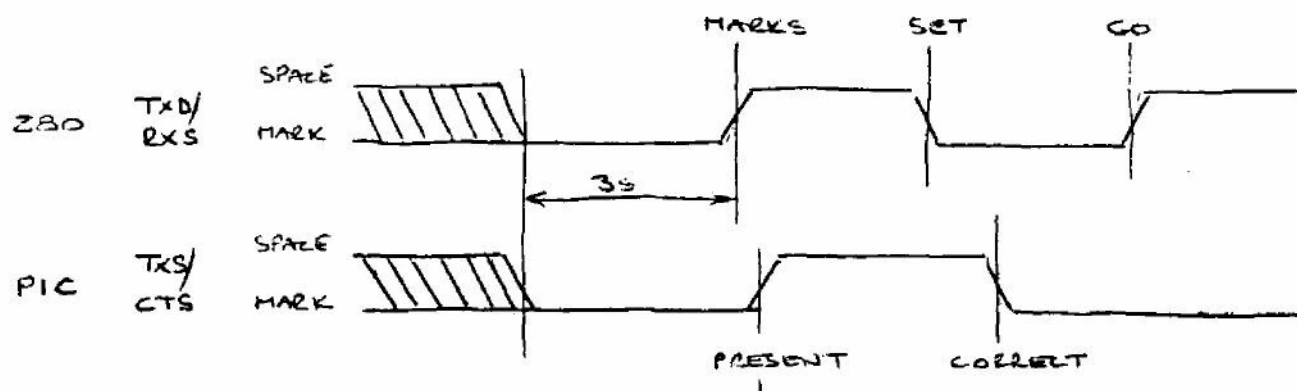
5.8 Keypad Scanning

5.8.1 The keypad (Figure 1.7) **comprises** a 5 x 4 switch matrix and a peripheral interface controller (PIC) with **on-chip** program and **scratchpad** memories. The PIC operates from a +5V rail derived by a simple stabiliser from the +12V Spectrum supply, and is clocked from an external LC network. The nominal **clock frequency** is 2.556 MHz but may vary between 1.278 MHz and 3.835 MHz dependent on component **tolerances**. The master clear input (MCLR) is active for a period after power-up or if the +12V supply is **temporarily** disconnected.

5.8.2 A two part protocol first synchronises the PIC with the Z80 after power up (or if the flex cable connection is temporarily broken) and then supports the transfer of keystroke data. Assuming synchronisation has been achieved (see below) the keypad scans the keypad once every other interrupt on demand **from the Z80**.

5.8.3 The keypad scanning routine is much the same as the routine adopted by the Z80 and ULA when scanning the main keyboard. The PIC addresses each column in turn and scans the rows to determine whether a key is pressed. The results of the scan are logged and passed to the Z80 on a demand/response basis (see para. 5.8.9). Each demand prompts the PIC to scan a row and report any change in the status **since** the previous scan. If there is no change, the PIC responds **negatively**, sending a space in response to the START signal from the Z80. In this case the PIC and Z80 determine that the next START signal is a call for the **result** of the row scan at the next **column** address. If the scan indicates that there has been a change in status since the previous scan, the PIC responds positively by sending a mark in response to the START **signal**. The Z80 responds by sending a further four START **signals**, prompting the PIC to transmit a 4-bit serial code with a '1' set in the bit position corresponding with the particular row. Since the Z80 keeps a log of the column address by counting the number of START signals it sends and registering the PIC responses since the start of the interrupt, it can readily identify the key code from a look-up **table**.

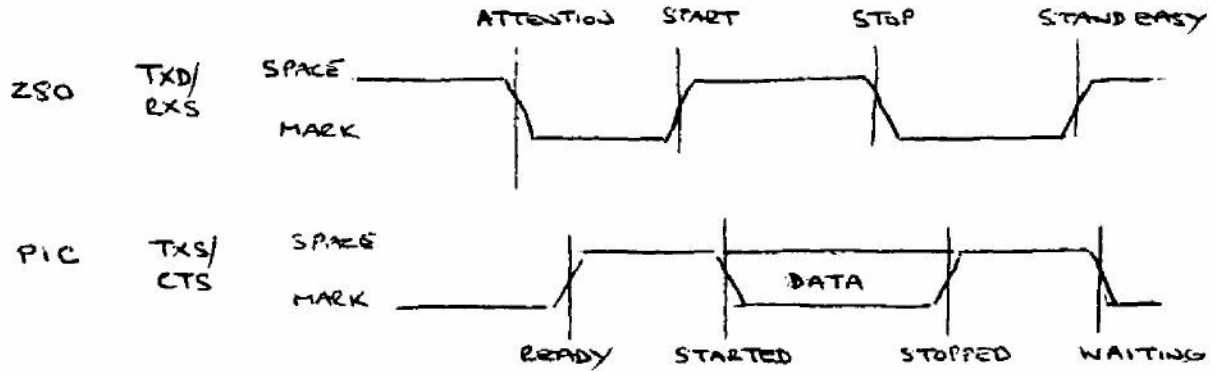
- 5.8.4 On a physical level, data exchanges between the PIC and the Z80 are conducted at RS232 signal levels over a single line pair - a transmit line (TXD/RXS) from the Z80 to the PIC and a receive line (CTS/TXS) from the PIC to the Z80. The transmit signal, originated by the Z80, is output as bit A0 from the Port A Data Store in the sound generator IC32 during a write to I/O address BFFD_H. From IC32 the data is converted from logic to RS232 levels in IC33 and routed from there to the PIC. A 4.3V zener diode on the keypad receive line, limits the positive signal excursion (space) to +4.3V and the negative signal excursion (mark) to 0V.
- 5.8.5 The transmit signal, originated by the PIC, follows a reciprocal path and is input to the Z80 from the sound generator as bit A5 in the Port A Data Store during a read from I/O address FFFD_H (NOTE: The RS232C receiver IC34 recognises a mark as 0V and a space as any level exceeding +3V).
- 5.8.6 Accesses to the Port A Data Store are identical to those described under the heading 'RS232/MIDI Interface'.
- 5.8.7 Reset Protocol. The synchronising sequence which runs after power up or reconnection (as seen at the RS232 connector) is shown below:



- 5.8.8 The significant time delays are as follows:
- The initial 3 second delay which ensures that the PIC is up and running. During this time the keypad is inoperative.
 - The 1ms delay between the Z80 setting TXD high (MARKS) and the PIC responding by setting TXS high (PRESENT). If the delay is exceeded, the Z80 assumes that some other device is connected, and abandons the reset sequence.

- c) The 0.6ms delay between the PIC returning to the idle state (CORRECT) and the Z80 setting TXD high (GO). If the delay is exceeded the keypad assumes that the Z80 has been reset and resets itself (i.e. returns to the start of the sequence).
- d) The 1 ms delay between the Z80 setting TXD high (SET) and the PIC responding by **putting** TXS low (CORRECT). If the **delay** is exceeded, the Z80 assumes that **some** other device is connected, and abandons the reset sequence.

5.8.9 Bit Transfer **Protocol**. The protocol for transferring a single bit from the PIC to the Z80 (as seen at the RS232 connector) is shown below:



5.8.10 The significant **levels** and time delays are as follows:

- a) At the start of the transfer the Z80 **polls** TXS which **should** be idling low. If not the Z80 assumes that some other device is connected and abandons the transfer.
- b) Having detected that TXS is low the Z80 sets TXD low (ATTENTION) and waits for the PIC to respond with **READY**. If **READY** is not received within 15 ms, the Z80 assumes that the keypad has been disconnected and abandons the transfer.
- c) After setting **READY** high the PIC polls RXS waiting for **START**. If not received within 0.2 ms the PIC assumes that the Z80 has been reset, and resets itself.
- d) On receiving **START** the PIC leaves TXS high if it wants to send a zero data bit, or puts it low to send a **'1'** (**STARTED**).
- e) Having received the data bit the Z80 sets TXD **low** (**STOP**); the PIC responds with TXS high, if not **already** so (**STOPPED**).

- f) Having responded with STOP, the PIC waits for the Z80 to set TXD high (STAND EASY); the PIC responds by setting TXS **low ready** to transfer the next data bit. If the **Z80** does not respond with STAND EASY within 1.3 ms the PIC assumes that the Z80 has been reset, and resets **itself**.
6. POWER SUPPLIES
- 6.1 The on-board power **supply** unit receives a 9V unregulated supply from the **external Sinclair ZX** power pack and derives the following internal supply rails:
- a) regulated +5V for the IC logic circuits, the ULA and the **sound/UHF** modulators
 - b) -5V for the expansion port
 - c) +12V for the RS232 driver IC33 and the keypad
 - d) -12V for the RS232 driver IC33 (unregulated -5V to -12V).
- 6.2 The **external** power pack incorporates a mains transformer, full wave rectifier and capacitive smoothing. A thermal fuse is fitted at the transformer input.
- 6.3 The on-board power supply unit (Figure 1.5) incorporates a 7805 regulator, deriving the +5V power **rail**, and an input supply for the inverter stage TR4/TR5. The latter raises the level of the +9V **unregulated** supply above +1 V. The resultant square wave at the junction of TR4 collector and the inverter coil is subsequently rectified and smoothed by 015/C44 producing the +12V output. The square wave at TR4 collector also supplies a charge pump C111/112 and D28,29 which derives the -12V rail. The **-8V** supply is taken from this **rail** via a zener D19.
- 6.4 The following supplies are available on the expansion connector:
- a) +5V (pin 3A)
 - b) pulsed +12V (pin 23B)
 - c) +12V (pin 23A)
 - d) -5V (pin 20B)
 - e) +9V unregulated (pin 4A)
 - f) ground (pins 6A, 7A, 14A)

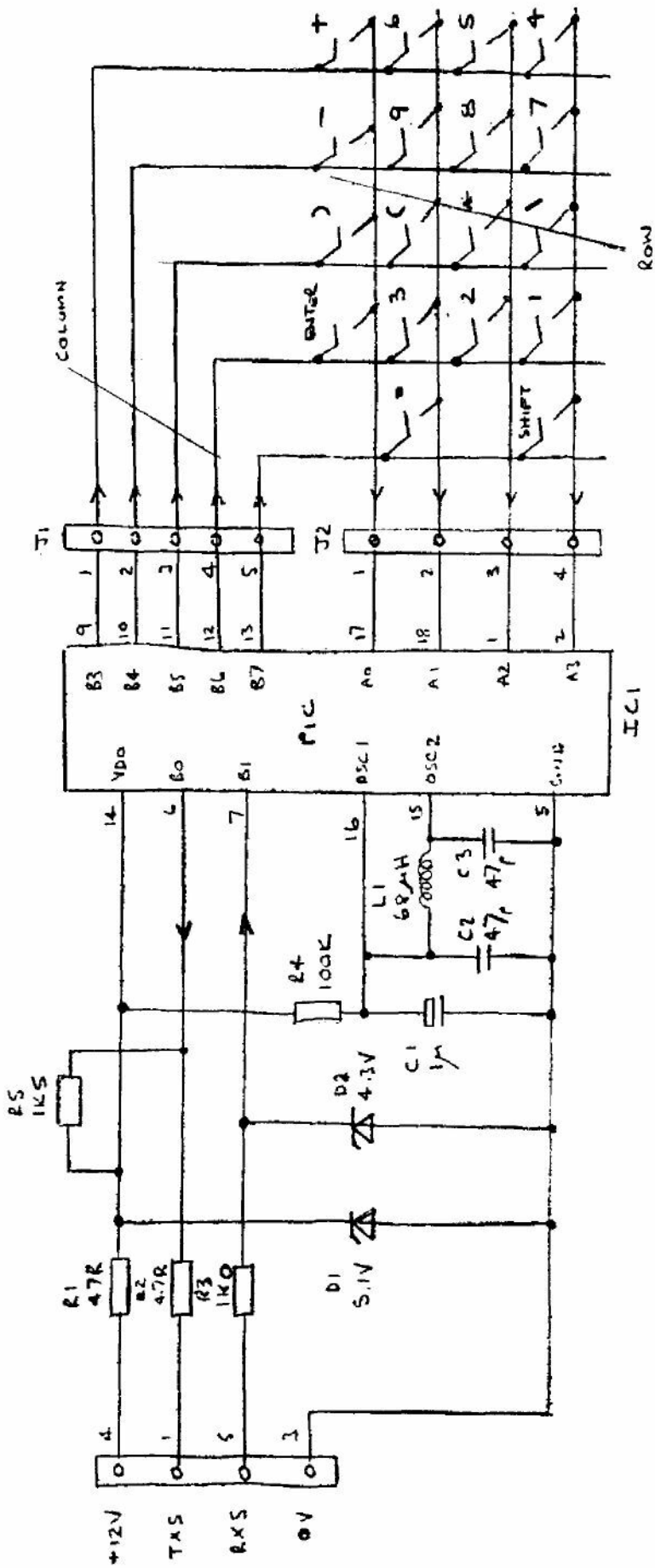


FIG 1.7 KEYPAD CIRCUIT

SECTION 2

DISASSEMBLY/ASSEMBLY

Sub-Section	LIST OF CONTENTS	Page No
1	Disassembly	2.1
2	Assembly	2.1

1. DISASSEMBLY

1.1 Unplug all input/output connectors and turn the computer upside down to reveal eight fixing screws. Release the screws (noting the position of two countersunk screws for re-assembly), turn the computer right side up and separate the case halves. To disassociate the case halves, carefully disconnect the keyboard ribbon cables from the pcb.

1.2 To remove the pcb from the lower case half remove the board fixing screws and the fixings securing the voltage regulator to the finned heatsink.

CAUTION If the pcb is to be powered-up when separated from the case, the pcb, with heatsink attached, should be removed as a complete assembly. The heatsink is secured to the case by two screws. Take care not to damage the electrical connections to the regulator.

1.3 To change the keyboard membrane, bubble mat or any of the keys, remove the membrane tail clamps followed by ten screws securing the keyboard reaction plate. Lift the plate clear followed by the membrane and bubble mat below. Individual keys can be removed for cleaning by pressing the key and gently prising the retaining sleeve off the underside of the key using a small screwdriver inserted under the rim.

2. ASSEMBLY

2.1 Assembly is generally carried out using the reverse procedure to that of disassembly. Do not overtighten the self-tapping fixing screws.

- 2.2 When replacing the keyboard components support the upper case half face down so that the keys are clear of the work surface. Position the bubble **mat**, membrane and reaction plate so that the **hole** at either end engages with the locating peg. Secure the fixing screws starting with the centre row. Tighten fully and back-off a 1/4 turn.
- 2.3 When clamping the membrane **tails** ensure that there is good **electrical** contact between the middle, upper and lower **tracks**. This is achieved by correctly positioning the packing pieces (extensions of the bubble mat) and ensuring that the ends of the middle tracks protude 1mm beyond the clamps. On new membranes, to prevent the possibility of short circuits, bond the upper and **lower** tracks together, close to the edge connector end, using double **sided tape**.
- 2.4 When **replacing** the **pcb**, ensure that the reset pushbutton is correctly located in the cut-out provided in the end of the case.
- 2.5 Before final assembly reconnect the keyboard ribbon **cables** (they should **lie** in an 'S' shape) and ensure that the legs and leg springs are in position.

SECTION 3

SETTING UP AND SYSTEM TEST

Sub-Section	LIST OF CONTENTS	Page No
1	Setting Up Instructions Sound Carrier Frequency	
2	System Test	

1. SETTING UP INSTRUCTIONS

TBD

2. SYSTEM TEST

TBD

3.1

SR1AAA

SECTION 4

FAULT FINDING AND REPAIR

Sub-Section	LIST OF CONTENTS	Page No
1	Introduction	4.1
	Test Equipment	4.1
2	Fault Diagnosis	4.2
	Techniques	4.2
	Power Supply Unit	4.3
	Initialisation	4.3
	Symptomatic Faults	4.5
3	Repair	4.6
Fig	ILLUSTRATIONS	
4.1	Test Oscillograms	4.7/8

1. INTRODUCTION

1.1 Test Equipment

Section 4 is intended as a guide to fault diagnosis and repair of the SPECTRUM 128. It is assumed that users have a **reasonable** knowledge of **electronic** servicing, theory and standard **fault-finding** techniques and have access to the test equipment and tools required to carry out the task. The **table** below contains a **list** of the minimum recommended test equipment and materials.

EQUIPMENT	SPECIFICATION/MANUFACTURER
Storage Oscilloscope with x10 probe	Rise Time: 0.02 us/cm
Variable power supply unit	0 to 30V d.c
Mono cassette recorder	With RECORD and PLAYBACK facilities
Mains extension lead	'Safebloc' type
Multimeter	General pupose
Colour Television and Monitor	Open Market
ZX Printer	Sinclair
Test tape	
Blank tape	Open Market
Double-sided adhesive tape?	12mm and 6mm wide, Tesafix 959 (B.D.FTESA) or 3M equivalent)

Engineers who are already familiar with the Sinclair SPECTRUM+ will find some similarities in the SPECTRUM 128. The SPECTRUM 128, however, is a more sophisticated device with improved colour and sound circuitry.

2. FAULT DIAGNOSIS

2.1 Techniques

In a closed loop system such as a computer, because of the interdependence of numerous component parts, fault diagnosis is not necessarily straight-forward. In addition, because of the high speed cyclic operation, interpretation of any waveforms on control, data and address lines as being valid depends to a large extent on practical experience of the system. There are however, certain checks with valid waveforms and levels that can be carried out before substituting any integrated circuits. Experience has shown that the best method of intially checking waveforms and levels can be to compare with the same point in a known serviceable board. The following pages provide a basic fault-finding procedure and furnish a list of possible faults along with suggested ways of curing them.

4.2

With a **densely** populated board such as the SPECTRUM 128, a **careful** physical examination of the board can sometimes indicate an obvious fault. Burnt-out discrete components or an overheated track show up immediately, as do the attentions of an enthusiastic amateur. Bearing in mind the latter, short circuits caused by **hairline** solder '**splatter**' can be of several ohms resistance and can cause some very misleading fault symptoms.

Provided first principles are adhered to and a common-sense approach is adopted, it will be found after a short space of time that fixing a faulty Spectrum is very much a routine operation.

2.2 Power Supply Unit

The **unstablied** external power supply unit is a source of some problems. The design is such that, at minimum input voltage (215V a.c.) and 1.4A output, the voltage trough should not be less than 7.0V; at maximum input voltage (265V a.c.) and 600mA output, the voltage peak should be less than 13V.

2.3 Initialisation

At switch-on the computer should **automatically** '**initialise**' and produce a **clear** screen with the statement.

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displayed in the lower left section of the screen. This indicates that most of the system is working. If the SPECTRUM 128 does not initialise, carry out the **following** basic checks.

Basic Checks. It is difficult to be specific in a **fault-finding** guide because of the **large** variety of fault conditions which can occur, but the **following** procedure, starting with a table of checks set out in order of priority, **will** however **isolate** the major fault area. The **oscillograms** reproduced on pages 4.6 and 4.7 are measured at points referenced on the circuit diagrams.

FUNCTION	CIRCUIT REF	VOLTAGE/WAVEFORM
Voltage regulator input	+ve side of C50	+9V d.c ± 2.0V. At less than +7V the regulator may not operate correctly
Voltage regulator output	+ve side of C34 and IC15 pin 8	+5V d.c ± 0.25V; no discernable ripple

(continued)

4.3

FUNCTION	CIRCUIT REF	VOLTAGE/WAVEFORM
On-board power	IC33 pin 14	+12V d.c + 0.5V
supply outputs:	IC34 pin 1	-12V d.c + 3V, -7V
	D19 anode	-5V d.c
		Check the oscillograms at points (A) and (B)
Clock pulses:		
Crystal	IC37 pin 6	17.73447 MHz with no jitter; check the oscillogram at point (C)
Z80	IC2 pin 6	3.54689 MHz with no jitter; check the oscillogram at point (D)
Colour encoder	Id pins 46,47	8.8 MHz with no jitter

- 2.4 If the basic tests prove satisfactory check the +5V and ground distribution to the ROM, Z80, ULA and the RAM. Also check the following:
- The \overline{RD} , \overline{WR} , \overline{MREQ} , DO-D7 and AO-A15 lines from the Z80. They should **all** be active immediately following a reset.
 - The $\overline{RAS}/\overline{CAS}$ lines to the **uncontended** RAM area IC15-IC22. The lines should be active immediately **following** a rest.
 - The $\overline{RAS}/\overline{CAS}$ lines to the contended RAM area IC6 to IC13. Compare with the oscillograms at points (E) and (F). (The RESET pushbutton should be operated to obtain a clear trace).
 - The ROM IC5 is enabled by an active low **signal** at pin 20.
 - The bank register IC312 is loaded with the correct values. Immediately after reset, pins 2,5,7,10,12 and 15 should be **low**.
 - Check the outputs on the RGB connector.
 - Check the picture on a domestic **television** and **listen** for **keyclicks** each time the ENTER key is pressed. Also check the following:

- i) **LUMO** output on IC36 pin 7; compare with the **oscillogram** at point (G) on the circuit.
- ii) Sound carrier on IC38 pin 4; compare with the oscillogram at point H on the circuit. The frequency should be within **2** KHz of 6.0 MHz for U.K operation or 5.5 MHz for European operation. Adjust as per the Setting Up Instructions if the **tolerance** is exceeded.
- iii) Drive into the modulator; compare with the **oscillogram** at point (J) on the circuit. Note the d.c. **level** at the bottom of the waveform (**typically** 185 mV).

2.5 Symptomatic **Faults**

As with any complex digital equipment the possible permutations are vast, thus the **following** table is not intended to be an exhaustive list of the faults that might occur on the Spectrum. It is intended as a guide **only** to possible courses of action to follow when faults show up in particular areas of the circuit. These areas are listed in the table with sub-headings, in no particular order of priority. It is envisaged that the ZXTP test tape has been **loaded**, or an attempt has been made to load the tape, in order to check for a faulty condition.

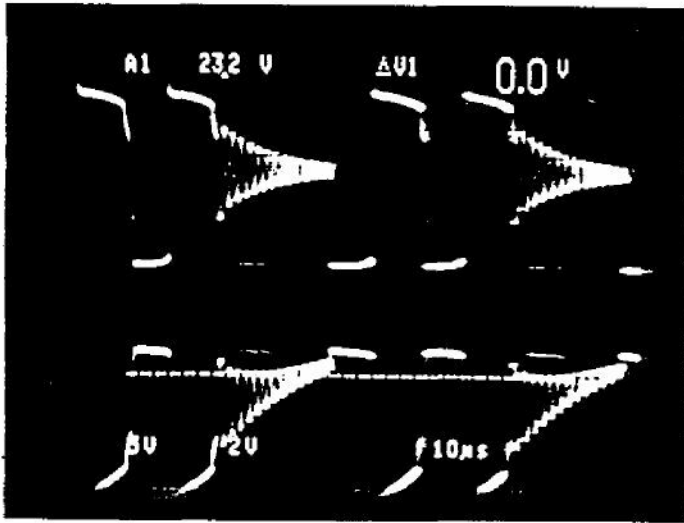
AREA		SYMPTON	ACTION
TBD		TBD	TBD

Authors Note: Table details to follow when **production** and in-service history is known.

3. REPAIR

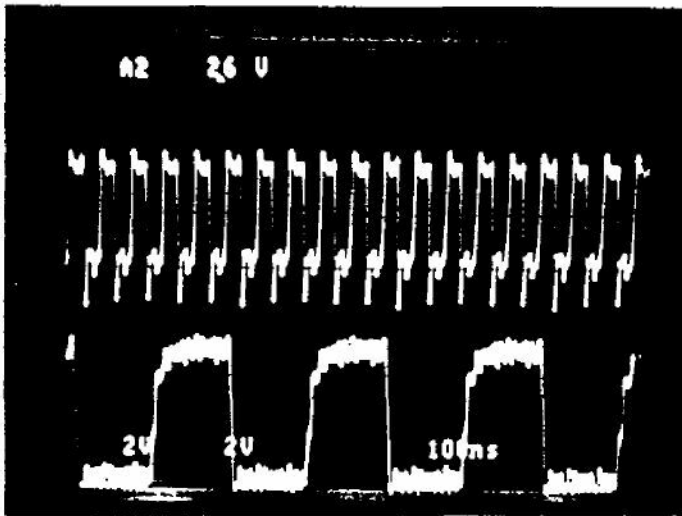
3.1 Renewal of components should be carried out using recognised desoldering/heatsinking techniques to prevent damage to the component or to the printed circuit board. Other points to be noted are:

- (a) When replacing a keyboard matrix, take care that the ribbon connectors are fully inserted into the board connectors, and are not kinked during insertion.
- (b) Make sure there is a good contact made between the voltage regulator body and the associated heatsink in order to ensure adequate heat conduction.
- (c) When the regulator is being replaced it is recommended that a suitable proprietary thermal grease is applied to the rear surface of the component body.
- (d) The modulator should be replaced as a complete unit.
- (e) When replacing plug-in ICs it is advisable to use the correct removal and insertion tools. Avoid contaminating the connection pins by handling.
- (f) When handling ICs take normal anti-static precautions. It is recommended that only a suitably earthed, low power soldering iron be used.
- (g) After any component has been renewed the circuit board should be examined carefully, to ensure that there are no solder 'splatters' which may cause short circuits between tracks and connector pins.



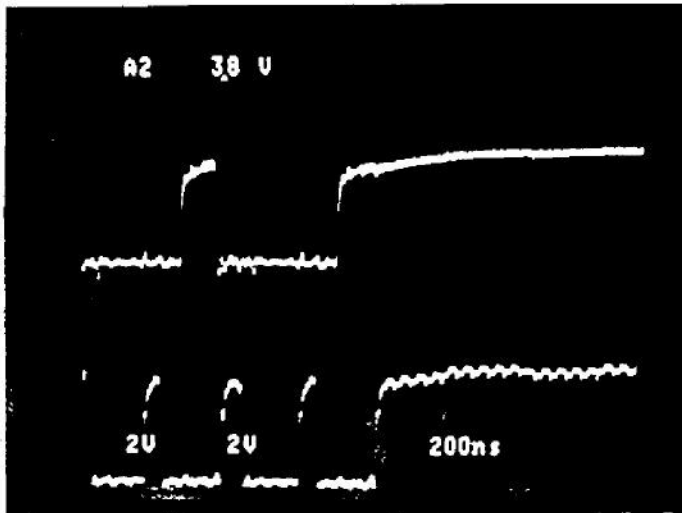
A (TR4 Collector)

B (TR4 Base)



C (IC37 Pin 6)

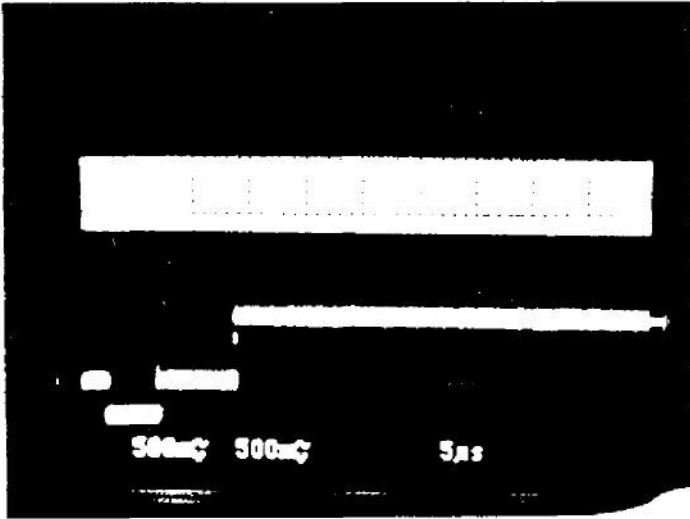
D (TR3 Collector)



E (Id Pin 42)

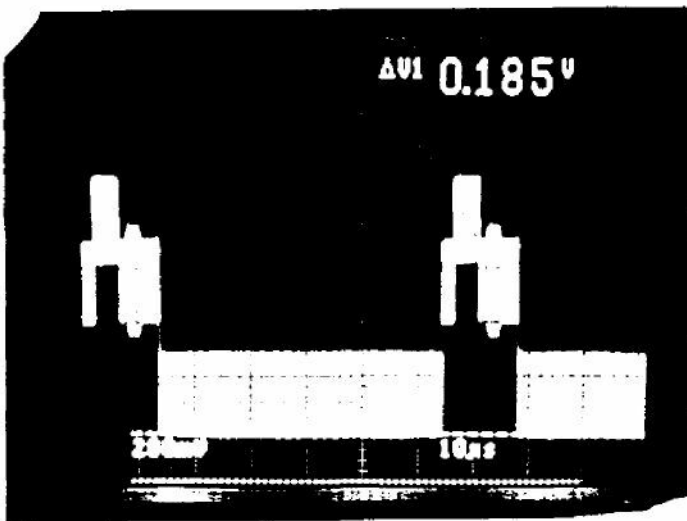
F (IC1 Pin 2)

FIG 4.1(A) TEST OSCILLOGRAMS (REF. FIGS 1.5 & 1.6)



C, (IC36 Pin 7)

H (IC38 Pin 4)



J (TR11 Emitter)

FIG 4.1(b) TEST OSCILLOGRAMS (REF. FIG. 1.6)

TABLE 5.2 MAIN PCB COMPONENTS

Circuit Reference	Value	Rating/ Tolerance	Manufacturer/ Type	Notes
CAPACITORS (Unless otherwise stated all capacitors are axial types)				
C1-C8	22nF	25V, 10%	Ceramic	
C9-C24	Not used			
C25	100uF	10V, -10%+80%	Electrolytic	
C26	22nF	25V, 10%	Ceramic	
C27	1uF	50V, 10%	Electrolytic	
C28	22uF	10V, -10%+80%	Electrolytic	
C29, 31	22nF	25V, 10%	Ceramic	
C31	100nF	25V, 10%	Ceramic	
C32	100nF	25V, 10%	Ceramic	
C33	Not used			
C34	22uF	10V, -10%+80%	Electrolytic	
C35	10nF	25V, 10%	Ceramic	
C36-C40	Not used			
C41	22nF	25V, 10%	Ceramic	
C42	Not used			
C43	100nF	25V, 10%	Ceramic	
C44, 45	100uF	10V, -10%+80%	Electrolytic	
C46-C48	Not used			
C49	560pF	25V, 10%	Ceramic	
C50	22uF	10V, -10%+80%	Electrolytic	
C51-C54	Not used			
C55-C62	22nF	25V, 10%	Ceramic	
C63-C65	Not used			
C66	22nF	25V, 10%	Ceramic	
C67	100pF	25V, 10%	Ceramic	
C68-C73	Not used			
C74	4.7uF	5V MIN	Electrolytic	
C75	100nF	25V, 10%	Ceramic	
C76-C79	Not used			
C80	22uF	10V, -10%+80%	Electrolytic	
C81-C99	Not used			
C100	10nF	25V, 10%	Ceramic	
C101	22nF	25V, 10%	Ceramic	
C102, 103	Not used			
C104	100nF	25V, 10%	Ceramic	
C105	180pF	25V, 10%	Ceramic	
C106-C110	22nF	25V, 10%	Ceramic	
C111, 112	47uF	16V, -10%+80%	Electrolytic	
C113 114	47nF	25V, 10%	Ceramic	
C115	330pF	25V, 2%	Ceramic	

Circuit Reference	Value	Rating/ Tolerance	Manufacturer/ Type	Notes
CAPACITORS (continued)				
C116	10nF	25V, 10%	Ceramic	
C117	Not used			
C118,119	1nF	25V, 10%	Ceramic	
C120	100pF	25V, 10%	Ceramic	
C121	47pF	25V, 10%	Ceramic	
C122	1nF	25V, 10%	Ceramic	
C123	1uF	10V, -10%+80%	Electrolytic	
C124	20pF	25V, 2%	Ceramic	(3)
C125	100nF	25V, 10%	Ceramic	
C126	22pF	25V, 10%	Ceramic	
C127	1uF	10V, -10%+80%	Electrolytic	
C128	47nF	25V, 10%	Ceramic	
C129	100pF	25V, 10%	Ceramic	
C130	(Note 6)	25V, 2%	Ceramic	(6)

COILS

Circuit Reference	Value	Rating/ Tolerance	Manufacturer/ Type	Notes
COIL	SPECTRUM TFR		N Devon	
L1/2			N Devon, Toroidal/ 2-winding	(7)
L3			Toko, 7KL (PF291ACS-1885Z)	
L4			Toko, 7KL (?)	(8)
L5	Not used			
L6,7	100uH		Taiyo, LAL04-0-101K	

CONNECTORS

Reference	Description	Manufacturer/Part No
EAR, MIC	3.5mm jack socket	TUDA
PWR	2.1mm co-axial socket	Hoseiden
KB1	5-way ribbon connector	BURNDY TE - 5 - 5S1V3
KB2	8-way ribbon connector	BURNDY TE - 8 - 5S1V3
RGB	8-way DIN socket or 9-way D-Type connector	
KEYPAD, RS232	6-way telephone jack socket	BICC, BT Type, 603A

CRYSTALS

Circuit Reference	Frequency	Manufacturer/Type	Notes
X1	17.734475 MHz		(5)

DIODES

Circuit Reference	Device	Manufacturer/Type	Notes
D1-D8	IN4148	Signal	
D9-D12	Not used		
D13	IN4148	Signal	
D14	Not used		
D15	BA157	Rectifier	
D16	Not used		
D17	BA157	Rectifier	
D18	Not used		
D19	BZY88C5V1	Zener	
D20-D27	IN4148	Signal	
D28, 29	BA157	Rectifier	
D30-034	IN4148	Signal	

INTEGRATED CIRCUITS

Circuit Reference	Device	Manufacturer/Type	Notes
IC1 (ULA)	7C001	Ferranti	
IC2 (CPU)	Z80A/u780	Zilog/NEC	
IC3, 4	Not used		
IC5 (ROM)	SPECTRUM 128	VTI	(4)
IC6-IC13	4164	150ns	(1)
IC14	Not used		
IC15-IC22	4164	150ns	(1)
IC23-IC26	Not used		
IC27	ZX8401	Mullard	
IC28	74LS04	Texas	
IC29	HAL10H8CN	MMI, National	
IC30	74LS157	Not National	
IC31	74LS174		
IC32	AY-3-8912A	General Instrument	
IC33	1488		
IC34	1489		
IC35	Not used		
IC36	TEA2000	Phillips	
IC37	74S04		
IC38	MC1376	Motorola	

RESISTORS (1/4W, 5% unless otherwise stated)

Circuit Reference	j	Value	Rating/ Tolerance	Manufacturer/ Type	Notes
1	R1-R8	470R			
j	R9-R16	8K2			
j	R17-R23	470R			
j	R24	1K0			(2)
j	R25	180R			
j	R26,27	470R			
	R28-R30	10K0			
1	R31	220K			
	R32	Not used			
	R33	680R			
	R34	15R	0.5W or 1W		
	R35	10K0			
	R36	680R			
	R37	1K0			
	R38-R57	Not used			
	R58	1K0	2%		
	R59	1K8	2%		
	R60	220R			
	R61	15R			
	R62-R64	Not used			
	R65-R67	10K0			
	R68	6K8			
	R69	10K0			
	R70-R72	Not used			
	R73	1K0			
	R74-R78	Not used			
	R79	2K2			
	R80-R86	Not used			
	R87	OR			
	R88	1K0			
	R89	8K2			
	R90	1K5			
	R91-R95	68R			
	R96-R98	10K0			
	R99	470R			
	R100	1K5			
	R101,102	820R			
	R103	3K3			
	R104	470R			
	R105	1K0			
	R106	820R			
	R107	3K9			
	R108	6K8			
	R109	4K7			
	R110	15K0			
	R111	39K0			

RESISTORS (Continued)

Circuit Reference	Value	Rating/ Tolerance	Manufacturer/ Type	Notes
R112	68K0			
R113	36K0	2%		
R114	1K0			
R115	10K0			
R116	Not used			
R117-R120	1K0			
R121	Not used			
R122	1K0			
R123	180R			
R124,125	470R			
R126	330R			
R127	1K5			
R128	8K2			
R129	1K0			
R130,131	1K5			
R132	39K0			
R133	56R			
R134	75R	0.5W		
R135	8K2			
R136	Not used			
R137	47R			
R138	470R			

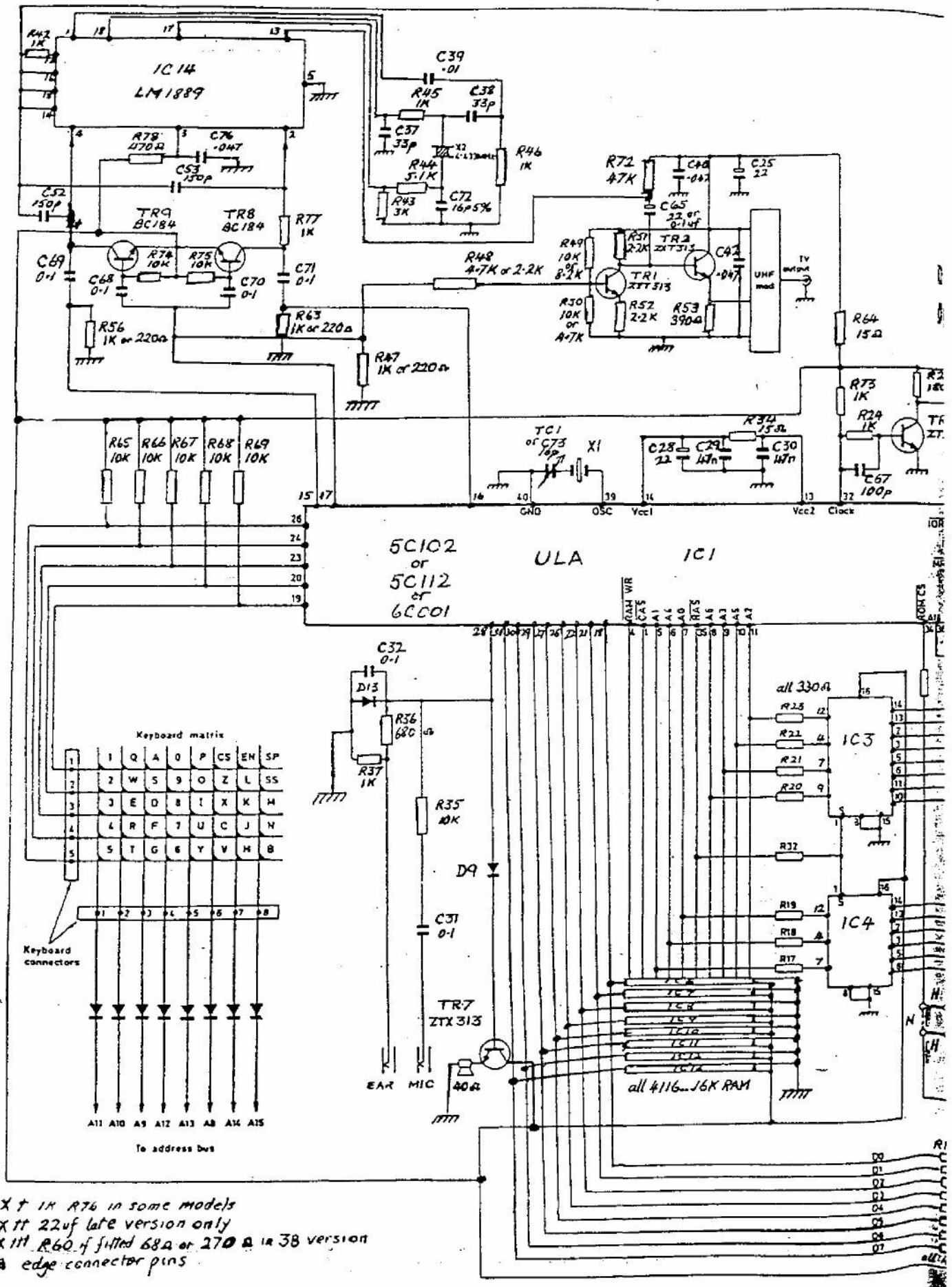
TRANSISTORS

Circuit Reference	Device	Alternative	Notes
TR1,2	Not used		
TR3	ZTX313	KSC839	(2)
TR4	ZTX650		
TR5	ZTX213		
TR6	ZTX313		
TR7	Not used		
TR8,9	Not used		
TR10	BC308B	8C213P/BC558B	
TR11-TR13	BC239B	8C184P/BC549B	
TR14	ZTX313		

TABLE 5.3 KEYPAD PCB COMPONENTS

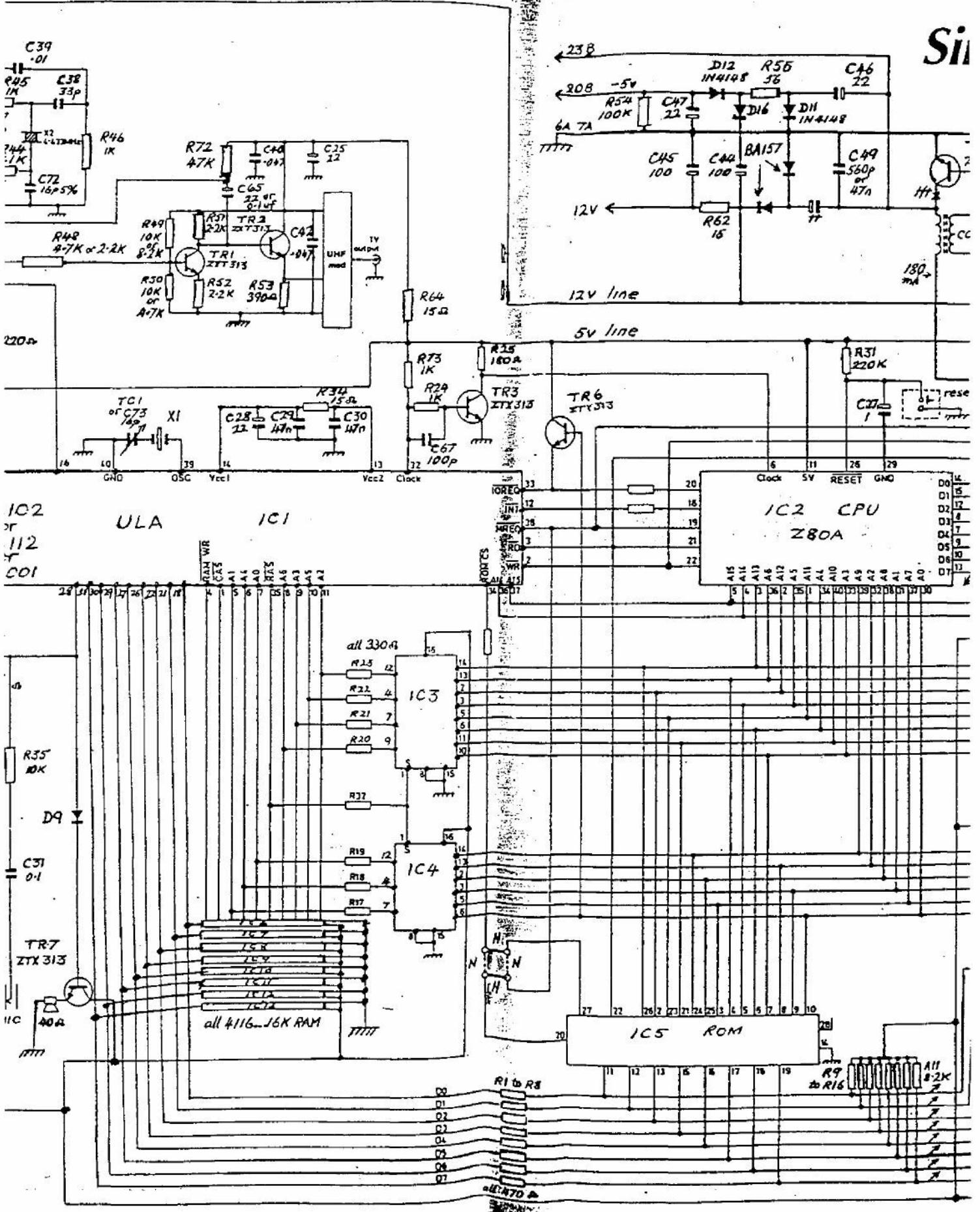
Circuit Reference	Value/ Descrip	Rating/ Tolerance	Manufacturer/ Type	Notes
CAPACITORS (axial types)				
C1	1uF	10V, -10%+80%	Electrolytic	
C2,3	47pF	25V, 10%	Ceramic	
COILS				
L1	68uH	+10%	Toko, 348LS - 680K	
CONNECTORS				
J1,2	5-way ribbon connector		BURNDY TE - 5 - 5S1V3	
J3	5-way connector		Molex, 4494-05-04	
DIODES				
D1	BZY88C	5V1	Zener	
D2	BZY88C	4V3	Zener	
INTEGRATED CIRCUITS				
Id	PIC1652		General Instrument	
RESISTORS (1/4W, 5%)				
R1,2	47R			
R3	1K0			
R4	100K			
R5	1K0			

NO	DESCRIPTION	PART NO.
1	I.C. Z80A/U780	X-1151
2	I.C. MULTIPLEXER 16 PIN	X-1152
3	I.C. PCF 1306P (ZX8401)	X-1153
4	I.C. 74LS04	X-1016
5	I.C. ROM-28 PIN 256K MASKX-1154	
6	I.C. ULA 7C001	X-1155
7	I.C. RAM 4164	X-1054
8	I.C. HAL10H8CN	X-1156
9	I.C. 74LS174	X-1157
10	I.C. AY-3-8912A	X-1158
11	I.e. 1488/MC1488P/SN 75188N	X-1067
12	I.C. 1489/SC1489P/SS 75189N	X-1068
13	I.e. TEA2000	X-1159
14	I.C. MC1376	X-1160
15	I.C. 74S04	X-1161
16	T.R. ZTX 313	X-1017
17	T.R. BC184P/BC239B/BC49B	X-1162
18	T.R. BC213/BC3088/BC5588	X-1163
19	T.R. ZTX 650	X-1164
20	DI. BA157	X-1023
21	DI. ZENER 500MW	X-1165
22	DI. IN4148	X-1022
23	COIL 5 PIN NEOSYD FORMER	X-1166
24	CHOKE BIFILAR WOUND	X-1167
25	COIL 7KL(6ohm)	X-1168
26	COIL 100 uH	X-1169
27	CRYSTAL 17.73447MHZ	X-1170
26	SOCKET ROM 28 PIN	X-1171
29	SOCKET EAR/MIC 3.5MM	X-1031
30	SOCKET POWER 3 LEG	X-1172
31	SOCKET U.L.A. 48 PIN	X-1173
32	SOCKET 3 WAY PIN	X-1174
33	SOCKET 6 VAY PIN	X-1175
34	CONNECTOR S WAY	X-1176
36	CONNECTOR b VAY	X-1177
MISCELLANEOUS		
36	MODULATOR U.K. TYPE	X-1178
37	LOVER CASE MOULDING	X-1179
38	KEYBOARD AND TOP CASE SUB ASSY	X-1180
39	RESET SWITCH SUB-ASSY	X-1181
40	FOOT RUBBER	X-1182
41	REACTION PLATE PLASTIC	X-1183
ACCESSORIES		
42	POWER SUPPLY 9V 1.85AMP UK 1850	X-1220
43	DATA TRANSFER CABLE 3.5MM3.5MM INTO-TWO	X-1203
44	128 SUPER TEST CASSETTE	X-1221
45	128 NEVER ENDING STORY CASSETTE	X-1222
46	R.F.CORD	X-1100
47	SERVICE MANUAL	X-1223
48	INTRODUCTION BOOK	X-1224
49	CARTON PLAIN + SA LABEL	X-1225
50	POLY PACK SET	X-1226/PP

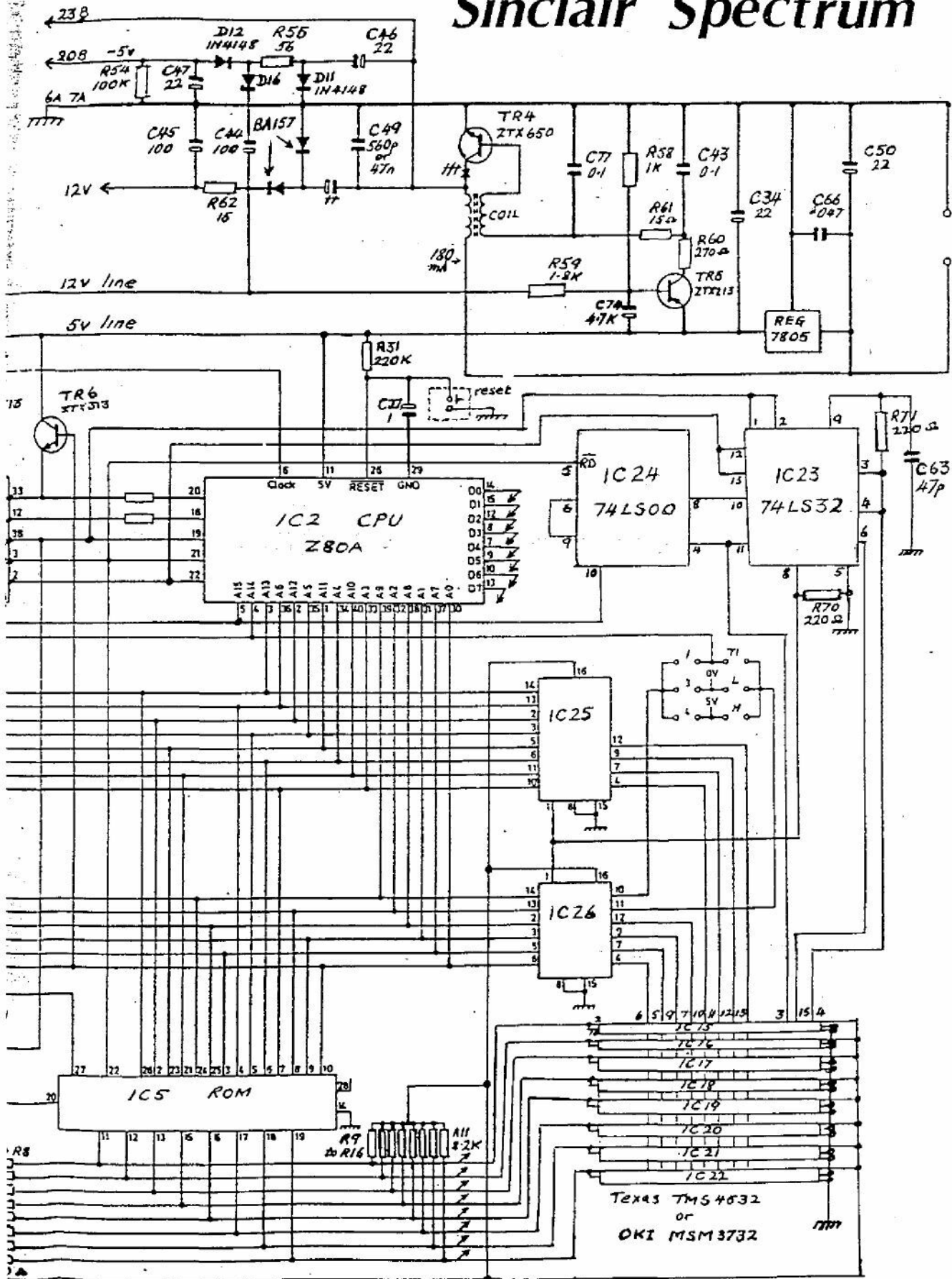


X† 1K R76 in some models
 X†† 22uf late version only
 X††† R60 of fitted 68Ω or 270 Ω in 3B version
 A edge connector pins

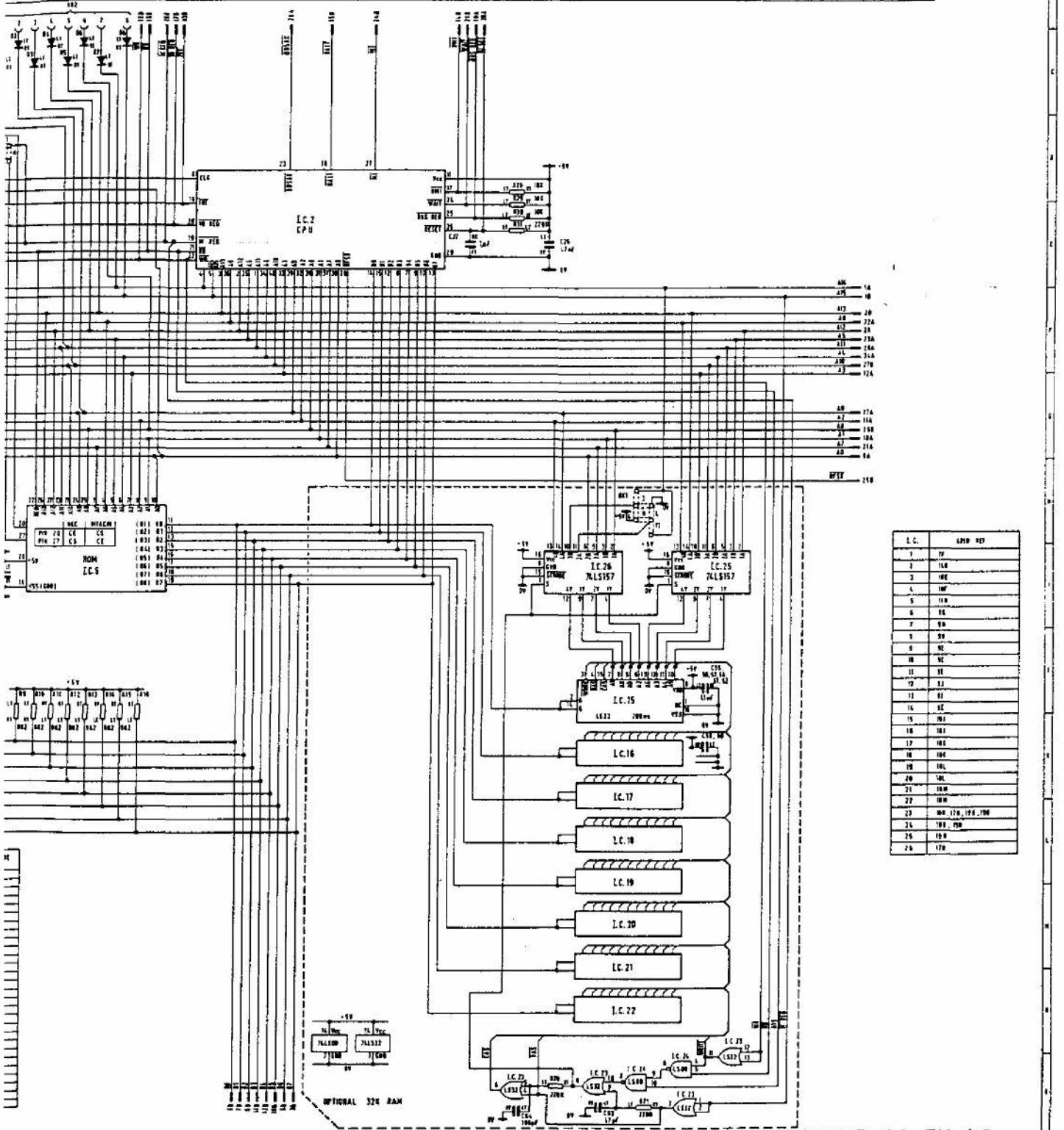
Sii



Sinclair Spectrum

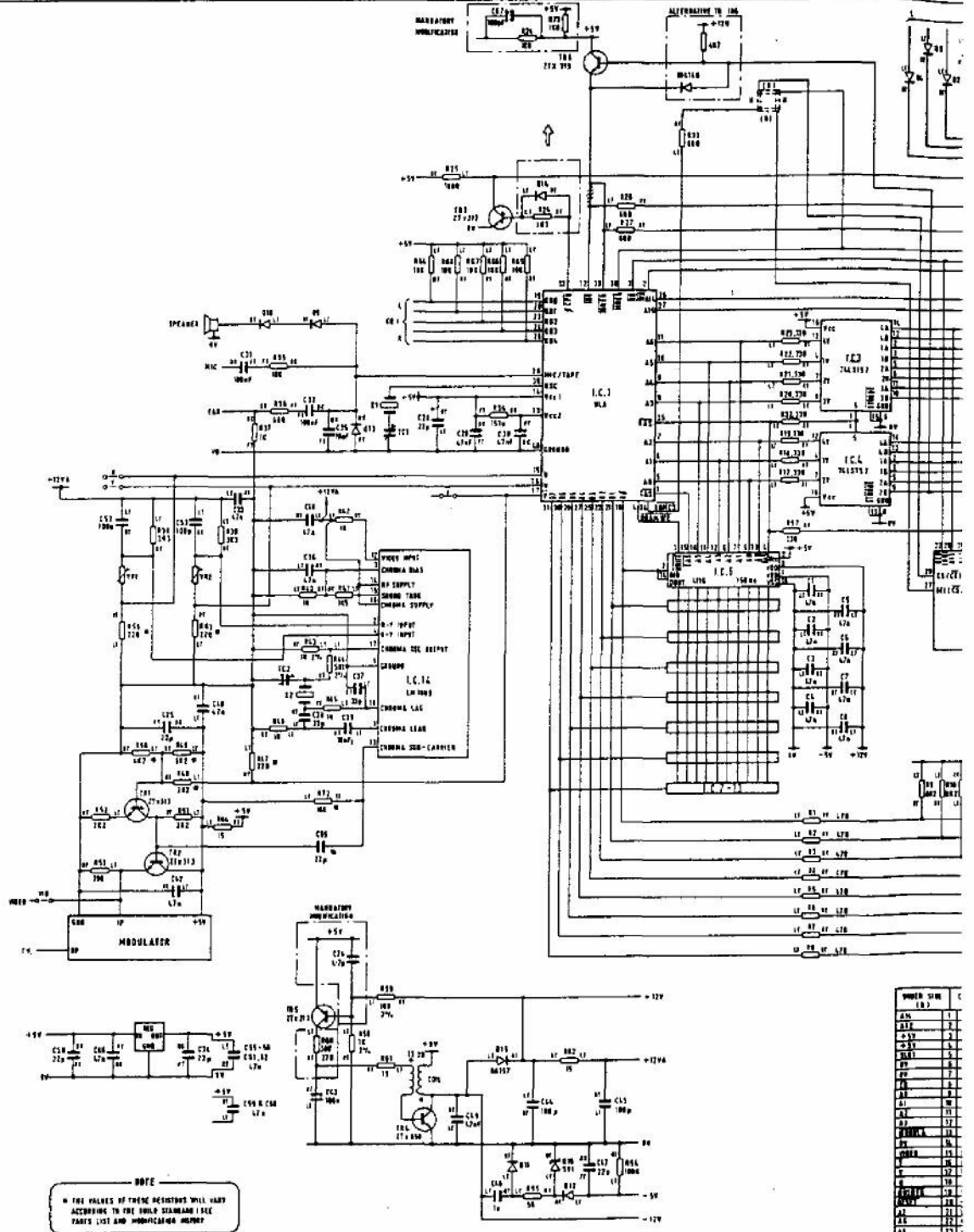


3, 4, 15, 12, 17, 16, 18, 19,	28, 29, 30, 31,	B
	27, 34, 26, 33,	C
1, 2, 5, 6, 7, 8,		F
		IV
1, COM. 102,	LINKS 101, 1, 1, 4, 8, 11,	MISC.



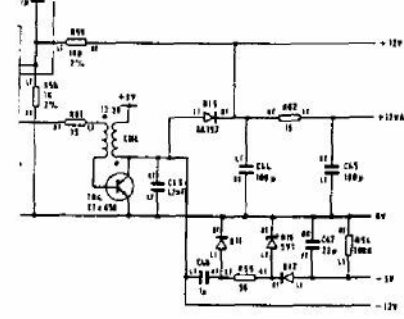
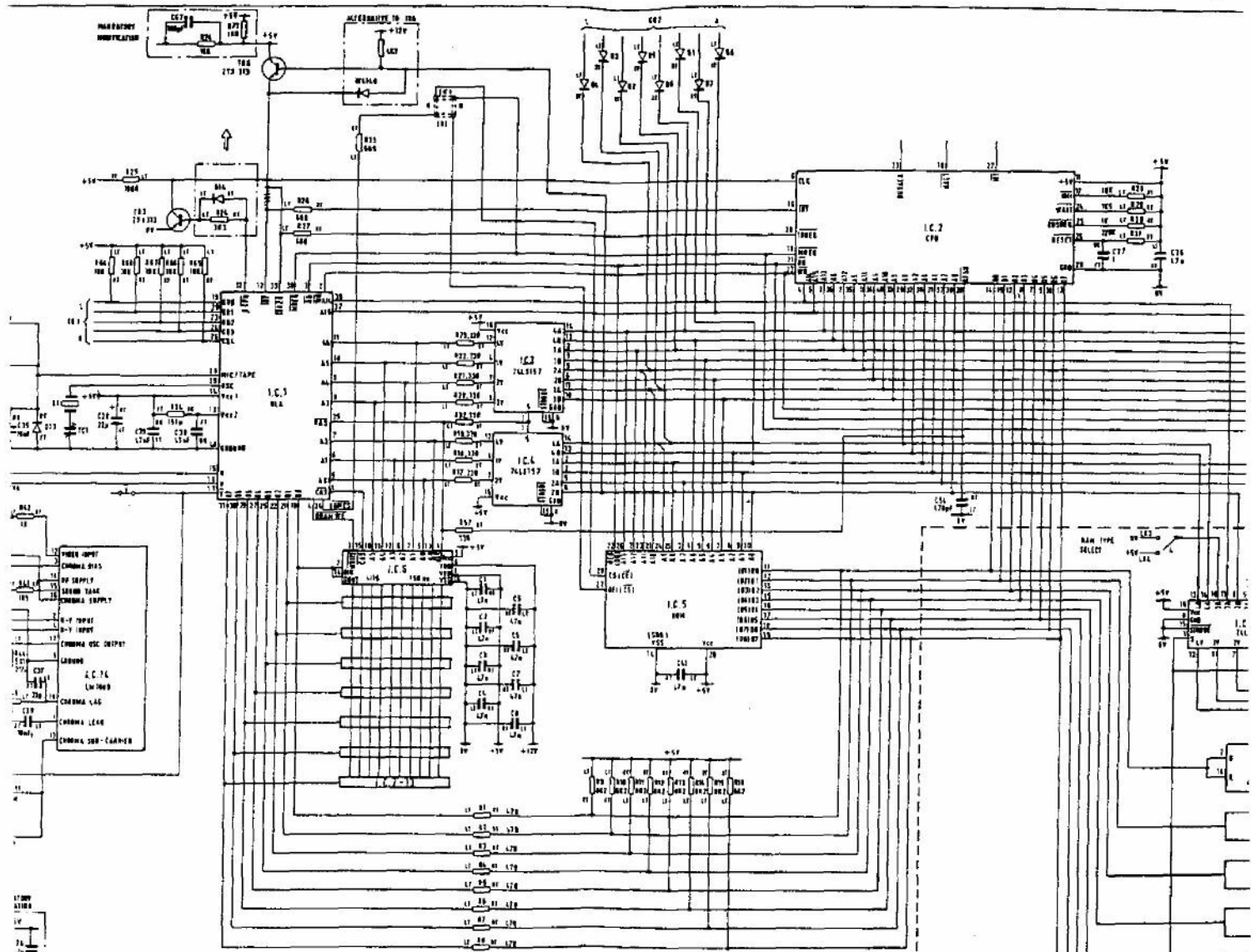
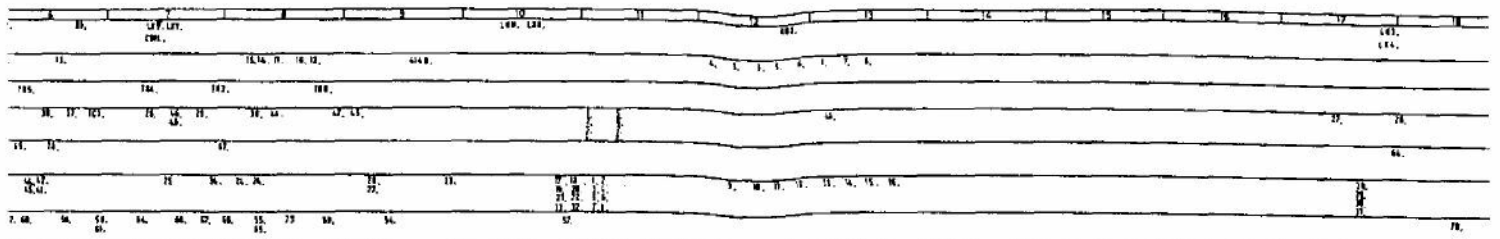
ZX SPECTRUM (ISSUE 3) FIG. 1.5
CIRCUIT DIAGRAM ESK12750
ISSUE A

74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200
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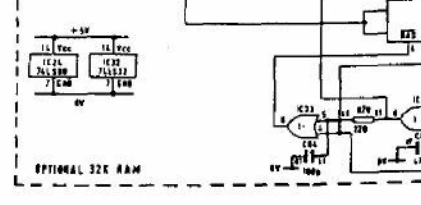


NOTE
 * THE VALUES OF THESE RESISTORS WILL VARY
 ACCORDING TO THE BUILT STANDARD I S E
 PARTS LIST AND MODIFICATION NUMBER

NUMBER	SYM	UNIT
1	10K	Ω
2	100K	Ω
3	100K	Ω
4	100K	Ω
5	100K	Ω
6	100K	Ω
7	100K	Ω
8	100K	Ω
9	100K	Ω
10	100K	Ω
11	100K	Ω
12	100K	Ω
13	100K	Ω
14	100K	Ω
15	100K	Ω
16	100K	Ω
17	100K	Ω
18	100K	Ω
19	100K	Ω
20	100K	Ω
21	100K	Ω
22	100K	Ω
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25	100K	Ω
26	100K	Ω
27	100K	Ω
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29	100K	Ω
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36	100K	Ω
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38	100K	Ω
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93	100K	Ω
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97	100K	Ω
98	100K	Ω
99	100K	Ω
100	100K	Ω



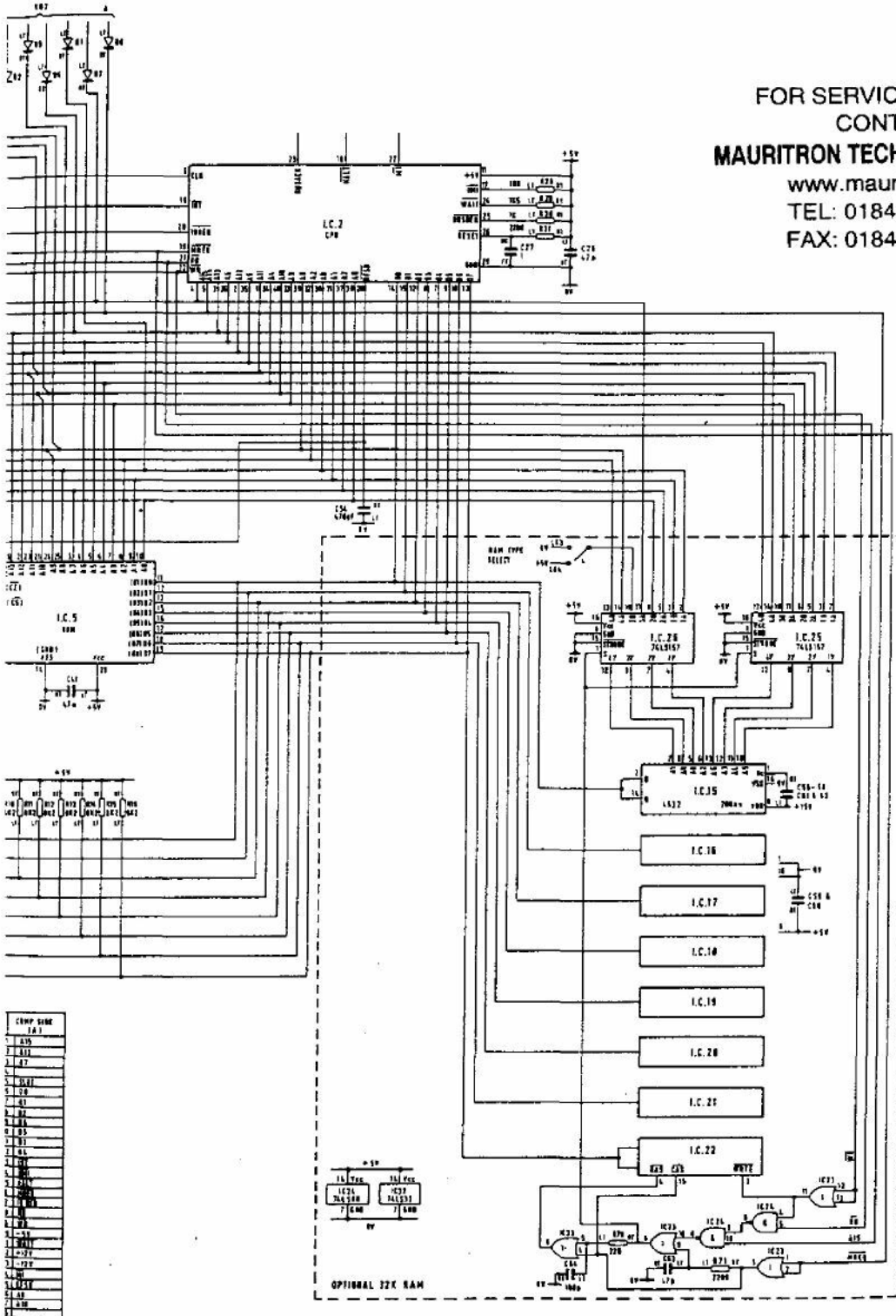
POWER SUPPLY	COMP. TYPE
1A1	1.5 100
1A2	1.5 100
1A3	1.5 100
1A4	1.5 100
1A5	1.5 100
1A6	1.5 100
1A7	1.5 100
1A8	1.5 100
1A9	1.5 100
1A10	1.5 100
1A11	1.5 100
1A12	1.5 100
1A13	1.5 100
1A14	1.5 100
1A15	1.5 100
1A16	1.5 100
1A17	1.5 100
1A18	1.5 100
1A19	1.5 100
1A20	1.5 100
1A21	1.5 100
1A22	1.5 100
1A23	1.5 100
1A24	1.5 100
1A25	1.5 100
1A26	1.5 100
1A27	1.5 100
1A28	1.5 100
1A29	1.5 100
1A30	1.5 100
1A31	1.5 100
1A32	1.5 100
1A33	1.5 100
1A34	1.5 100
1A35	1.5 100
1A36	1.5 100
1A37	1.5 100
1A38	1.5 100
1A39	1.5 100
1A40	1.5 100
1A41	1.5 100
1A42	1.5 100
1A43	1.5 100
1A44	1.5 100
1A45	1.5 100
1A46	1.5 100
1A47	1.5 100
1A48	1.5 100
1A49	1.5 100
1A50	1.5 100
1A51	1.5 100
1A52	1.5 100
1A53	1.5 100
1A54	1.5 100
1A55	1.5 100
1A56	1.5 100
1A57	1.5 100
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1A68	1.5 100
1A69	1.5 100
1A70	1.5 100
1A71	1.5 100
1A72	1.5 100
1A73	1.5 100
1A74	1.5 100
1A75	1.5 100
1A76	1.5 100
1A77	1.5 100
1A78	1.5 100
1A79	1.5 100
1A80	1.5 100
1A81	1.5 100
1A82	1.5 100
1A83	1.5 100
1A84	1.5 100
1A85	1.5 100
1A86	1.5 100
1A87	1.5 100
1A88	1.5 100
1A89	1.5 100
1A90	1.5 100
1A91	1.5 100
1A92	1.5 100
1A93	1.5 100
1A94	1.5 100
1A95	1.5 100
1A96	1.5 100
1A97	1.5 100
1A98	1.5 100
1A99	1.5 100
1A100	1.5 100



OPTIONAL 32K RAM

192.	193.	194.	195.	196.	197.	198.	199.	200.	201.	202.	203.	204.	205.	206.	207.	208.	209.	210.	211.	212.	213.	214.	215.	216.	217.	218.	219.	220.	221.	222.	223.	224.	225.	226.	227.	228.	229.	230.	231.	232.	233.	234.	235.	236.	237.	238.	239.	240.	241.	242.	243.	244.	245.	246.	247.	248.	249.	250.	251.	252.	253.	254.	255.	256.	257.	258.	259.	260.	261.	262.	263.	264.	265.	266.	267.	268.	269.	270.	271.	272.	273.	274.	275.	276.	277.	278.	279.	280.	281.	282.	283.	284.	285.	286.	287.	288.	289.	290.	291.	292.	293.	294.	295.	296.	297.	298.	299.	300.	301.	302.	303.	304.	305.	306.	307.	308.	309.	310.	311.	312.	313.	314.	315.	316.	317.	318.	319.	320.	321.	322.	323.	324.	325.	326.	327.	328.	329.	330.	331.	332.	333.	334.	335.	336.	337.	338.	339.	340.	341.	342.	343.	344.	345.	346.	347.	348.	349.	350.	351.	352.	353.	354.	355.	356.	357.	358.	359.	360.	361.	362.	363.	364.	365.	366.	367.	368.	369.	370.	371.	372.	373.	374.	375.	376.	377.	378.	379.	380.	381.	382.	383.	384.	385.	386.	387.	388.	389.	390.	391.	392.	393.	394.	395.	396.	397.	398.	399.	400.	401.	402.	403.	404.	405.	406.	407.	408.	409.	410.	411.	412.	413.	414.	415.	416.	417.	418.	419.	420.	421.	422.	423.	424.	425.	426.	427.	428.	429.	430.	431.	432.	433.	434.	435.	436.	437.	438.	439.	440.	441.	442.	443.	444.	445.	446.	447.	448.	449.	450.	451.	452.	453.	454.	455.	456.	457.	458.	459.	460.	461.	462.	463.	464.	465.	466.	467.	468.	469.	470.	471.	472.	473.	474.	475.	476.	477.	478.	479.	480.	481.	482.	483.	484.	485.	486.	487.	488.	489.	490.	491.	492.	493.	494.	495.	496.	497.	498.	499.	500.	501.	502.	503.	504.	505.	506.	507.	508.	509.	510.	511.	512.	513.	514.	515.	516.	517.	518.	519.	520.	521.	522.	523.	524.	525.	526.	527.	528.	529.	530.	531.	532.	533.	534.	535.	536.	537.	538.	539.	540.	541.	542.	543.	544.	545.	546.	547.	548.	549.	550.	551.	552.	553.	554.	555.	556.	557.	558.	559.	560.	561.	562.	563.	564.	565.	566.	567.	568.	569.	570.	571.	572.	573.	574.	575.	576.	577.	578.	579.	580.	581.	582.	583.	584.	585.	586.	587.	588.	589.	590.	591.	592.	593.	594.	595.	596.	597.	598.	599.	600.	601.	602.	603.	604.	605.	606.	607.	608.	609.	610.	611.	612.	613.	614.	615.	616.	617.	618.	619.	620.	621.	622.	623.	624.	625.	626.	627.	628.	629.	630.	631.	632.	633.	634.	635.	636.	637.	638.	639.	640.	641.	642.	643.	644.	645.	646.	647.	648.	649.	650.	651.	652.	653.	654.	655.	656.	657.	658.	659.	660.	661.	662.	663.	664.	665.	666.	667.	668.	669.	670.	671.	672.	673.	674.	675.	676.	677.	678.	679.	680.	681.	682.	683.	684.	685.	686.	687.	688.	689.	690.	691.	692.	693.	694.	695.	696.	697.	698.	699.	700.	701.	702.	703.	704.	705.	706.	707.	708.	709.	710.	711.	712.	713.	714.	715.	716.	717.	718.	719.	720.	721.	722.	723.	724.	725.	726.	727.	728.	729.	730.	731.	732.	733.	734.	735.	736.	737.	738.	739.	740.	741.	742.	743.	744.	745.	746.	747.	748.	749.	750.	751.	752.	753.	754.	755.	756.	757.	758.	759.	760.	761.	762.	763.	764.	765.	766.	767.	768.	769.	770.	771.	772.	773.	774.	775.	776.	777.	778.	779.	780.	781.	782.	783.	784.	785.	786.	787.	788.	789.	790.	791.	792.	793.	794.	795.	796.	797.	798.	799.	800.	801.	802.	803.	804.	805.	806.	807.	808.	809.	810.	811.	812.	813.	814.	815.	816.	817.	818.	819.	820.	821.	822.	823.	824.	825.	826.	827.	828.	829.	830.	831.	832.	833.	834.	835.	836.	837.	838.	839.	840.	841.	842.	843.	844.	845.	846.	847.	848.	849.	850.	851.	852.	853.	854.	855.	856.	857.	858.	859.	860.	861.	862.	863.	864.	865.	866.	867.	868.	869.	870.	871.	872.	873.	874.	875.	876.	877.	878.	879.	880.	881.	882.	883.	884.	885.	886.	887.	888.	889.	890.	891.	892.	893.	894.	895.	896.	897.	898.	899.	900.	901.	902.	903.	904.	905.	906.	907.	908.	909.	910.	911.	912.	913.	914.	915.	916.	917.	918.	919.	920.	921.	922.	923.	924.	925.	926.	927.	928.	929.	930.	931.	932.	933.	934.	935.	936.	937.	938.	939.	940.	941.	942.	943.	944.	945.	946.	947.	948.	949.	950.	951.	952.	953.	954.	955.	956.	957.	958.	959.	960.	961.	962.	963.	964.	965.	966.	967.	968.	969.	970.	971.	972.	973.	974.	975.	976.	977.	978.	979.	980.	981.	982.	983.	984.	985.	986.	987.	988.	989.	990.	991.	992.	993.	994.	995.	996.	997.	998.	999.	1000.
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FOR SERVICE MANUALS
CONTACT:
MAURITRON TECHNICAL SERVICES
www.mauritron.co.uk
TEL: 01844 - 351694
FAX: 01844 - 352554

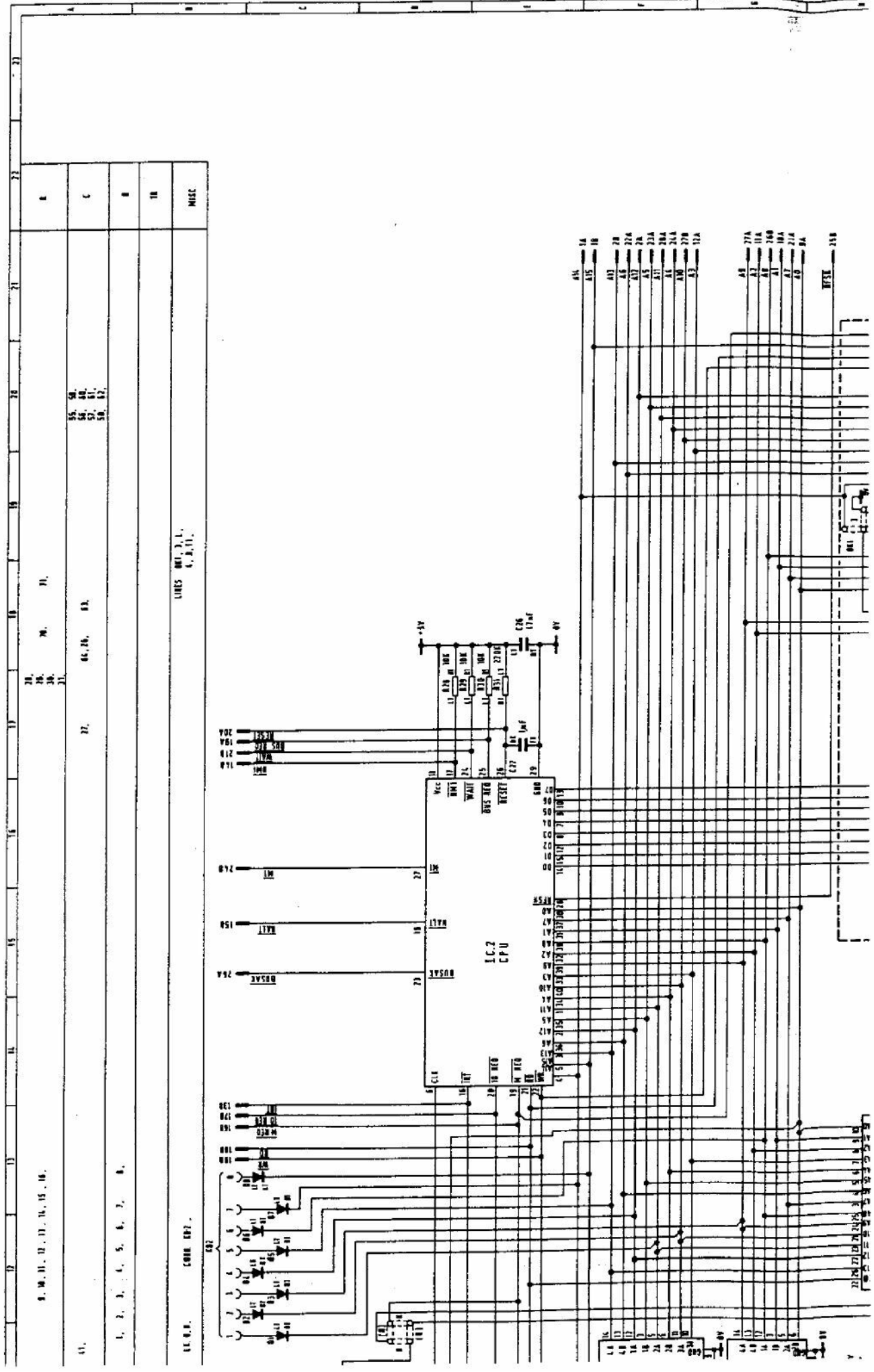


LAST IC No - IC26
LAST TEST No - 872
LAST GAP No - 600
LAST BOARD No - 204
LAST TRAYS No - 100
01-014 - 10-010
ALL OTHER REGISTRARS © S.M.

IC No.	MAN REF
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9	217, 211
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12	220, 211
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26	237

COMP SIDE

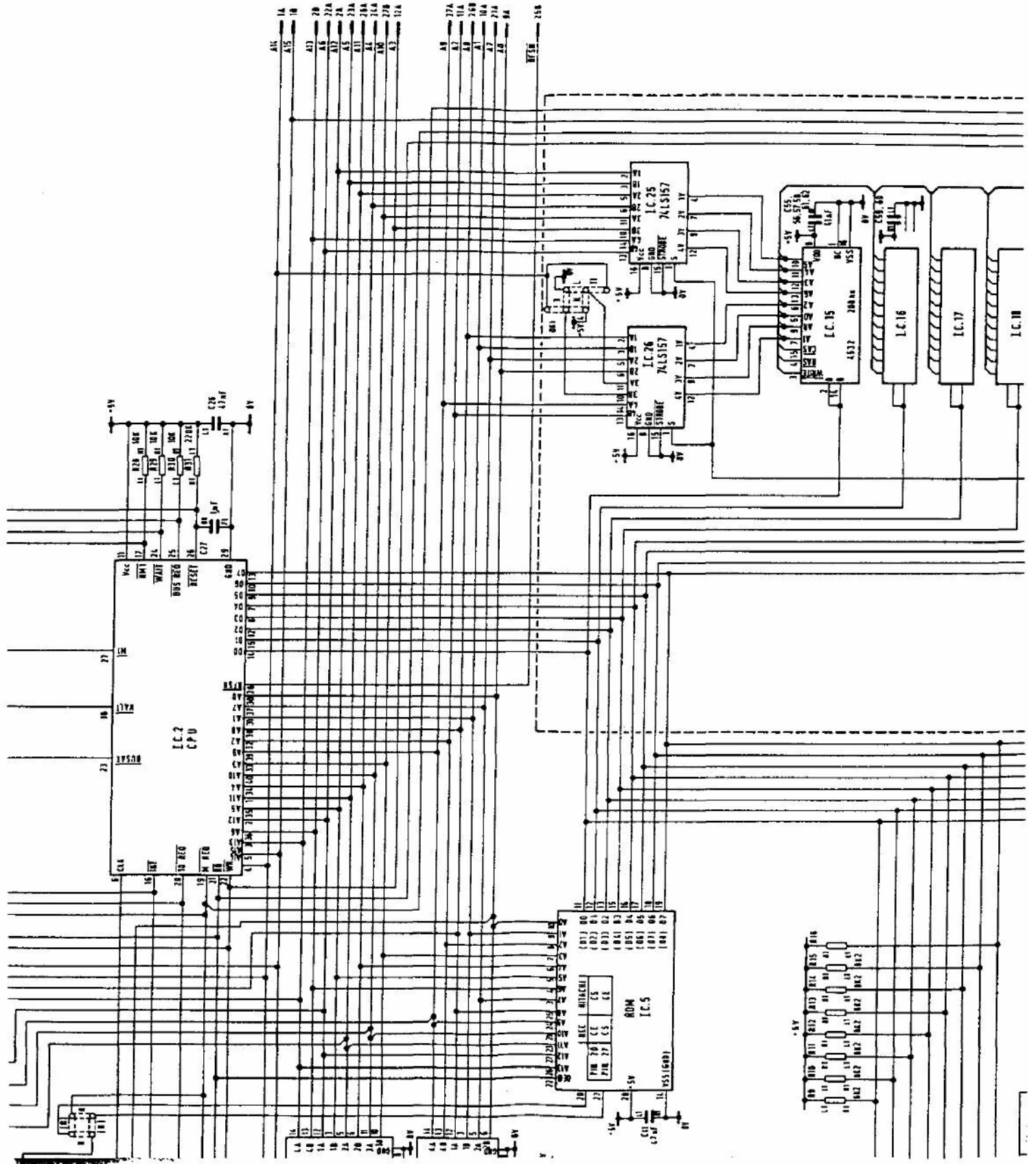
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U.S.P. COMM. DEPT.

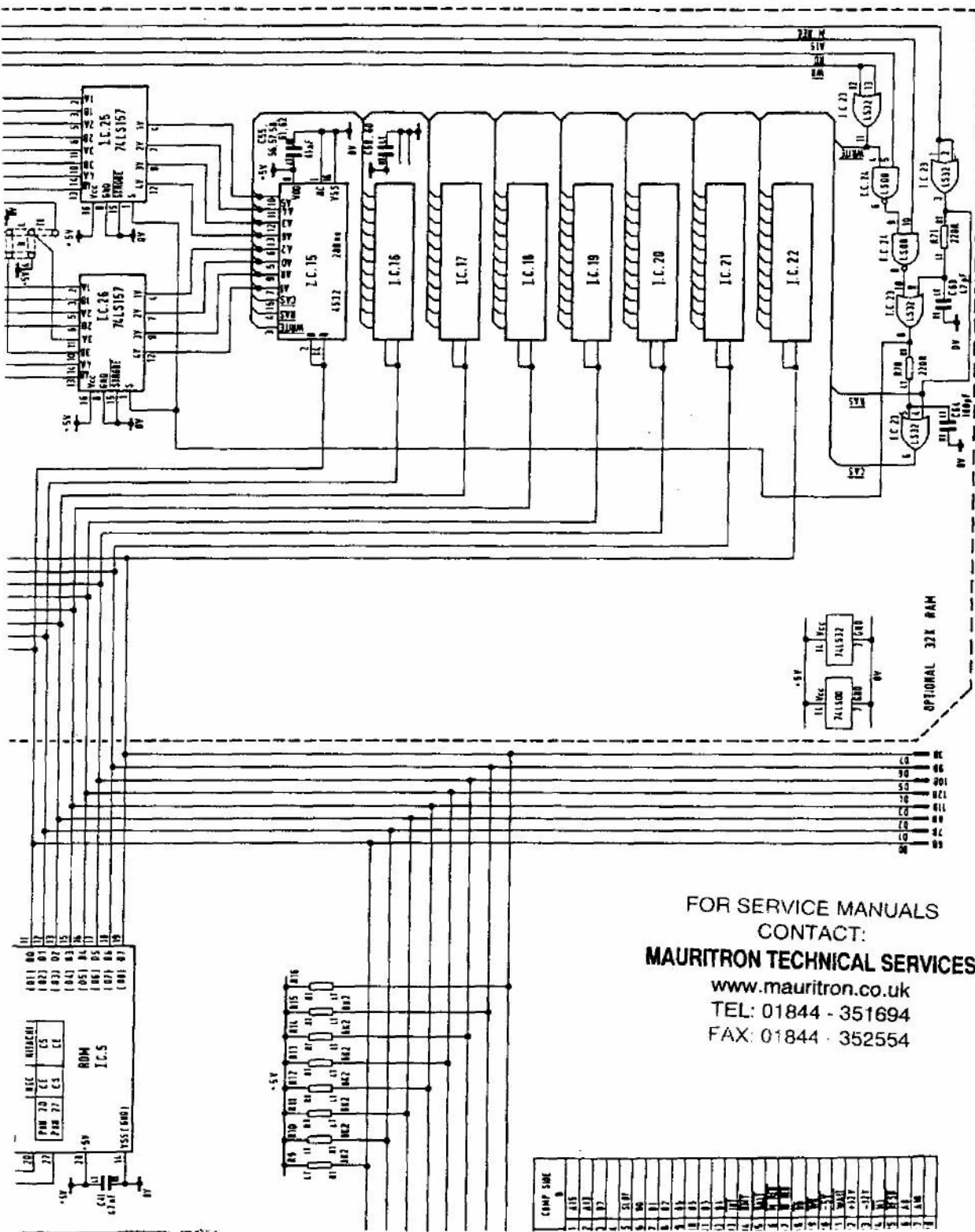
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1.	2, 3, 4, 5, 6, 7, 8.				



Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
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0010	01	01	01	01	01	01	01	01	01
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0000	01	01	01	01	01	01	01	01	01
1111	01	01	01	01	01	01	01	01	01
1110	01	01	01	01	01	01	01	01	01
1101	01	01	01	01	01	01	01	01	01
1100	01	01	01	01	01	01	01	01	01
1011	01	01	01	01	01	01	01	01	01
1010	01	01	01	01	01	01	01	01	01
1001	01	01	01	01	01	01	01	01	01
1000	01	01	01	01	01	01	01	01	01
0111	01	01	01	01	01	01	01	01	01
0110	01	01	01	01	01	01	01	01	01
0101	01	01	01	01	01	01	01	01	01
0100	01	01	01	01	01	01	01	01	01
0011	01	01	01	01	01	01	01	01	01
0010	01	01	01	01	01	01	01	01	01
0001	01	01	01	01	01	01	01	01	01
0000	01	01	01	01	01	01	01	01	01

I.C.	DATA REF.
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4	100
5	118
6	80
7	80
8	91
9	91
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11	91
12	91
13	91
14	61
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17	100
18	100
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20	101
21	100
22	100
23	MR 170, 181, 190
24	190, 190
25	190



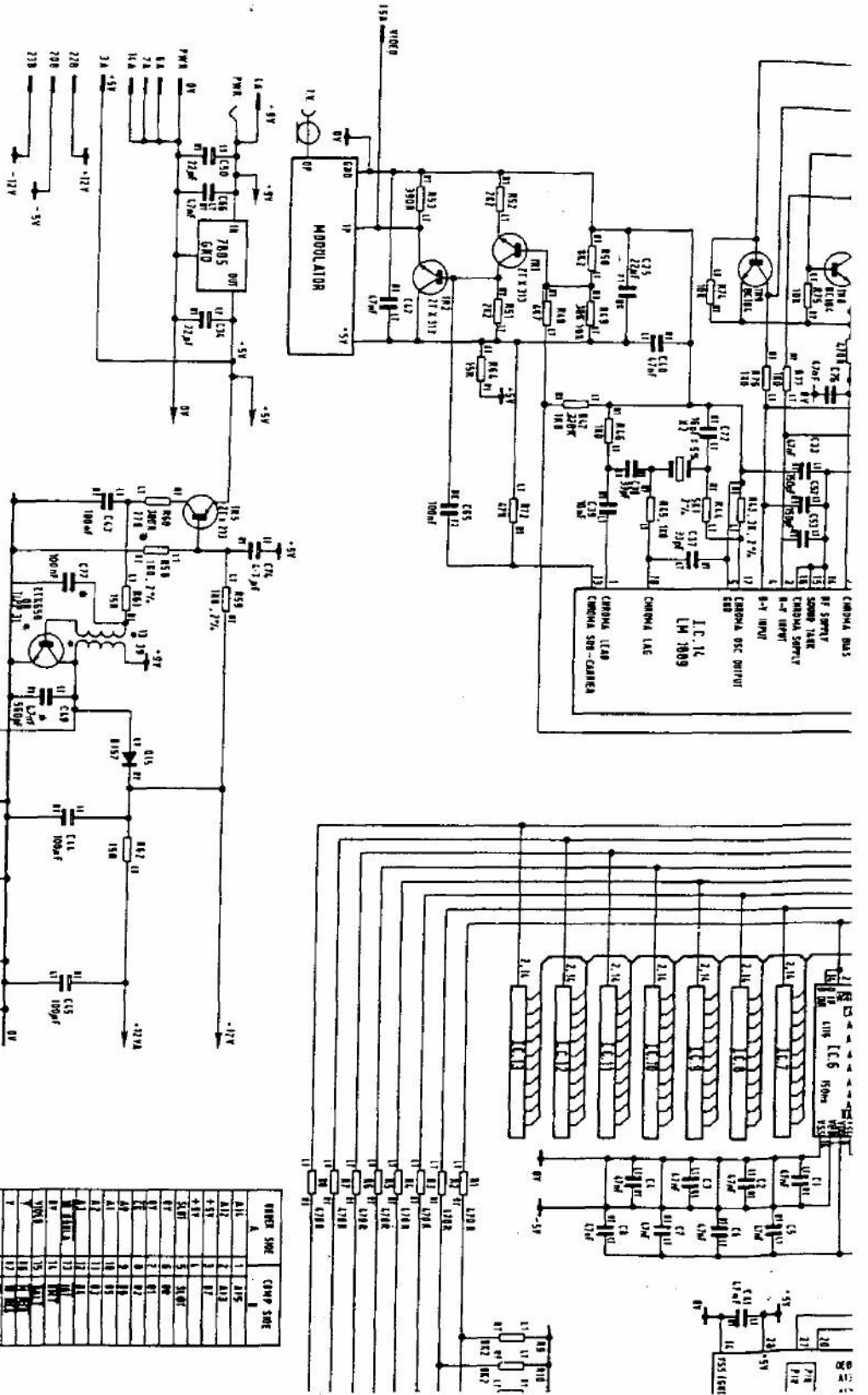
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5	11H
6	3E
7	3H
8	3H
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10	3E
11	3E
12	3E
13	3E
14	3E
15	3E
16	3E
17	3E
18	3E
19	3E
20	3E
21	3E
22	3E
23	3E
24	3E
25	3E
26	3E

IC	GRID REF
1	2F
2	14G
3	10E
4	10F
5	11H
6	3E
7	3H
8	3H
9	3E
10	3E
11	3E
12	3E
13	3E
14	3E
15	3E
16	3E
17	3E
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19	3E
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22	3E
23	3E
24	3E
25	3E
26	3E

COMP	SHR
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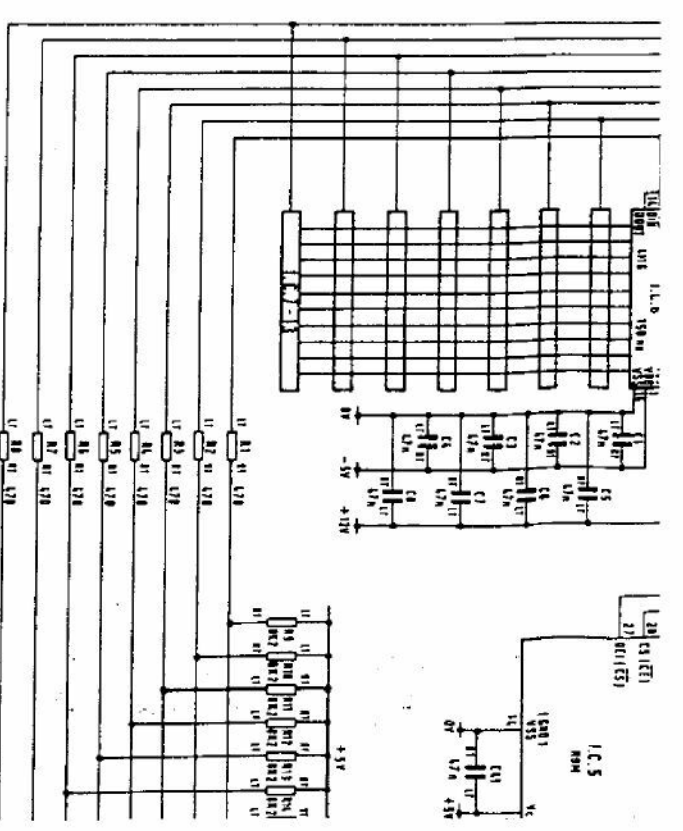
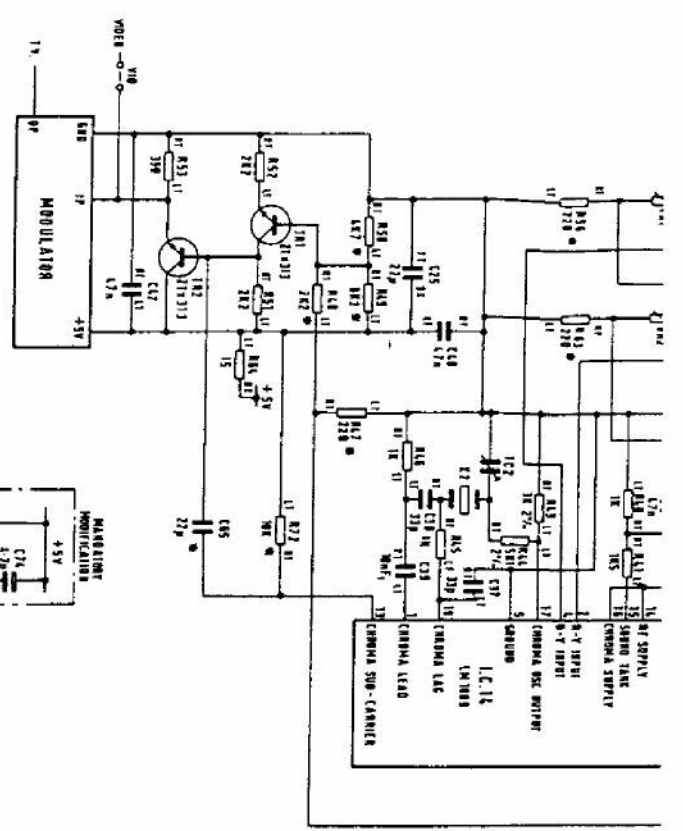
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ZX SPECTRUM (ISSUE 3) FIG. 1.5
CIRCUIT DIAGRAM ESK12750
ISSUE A

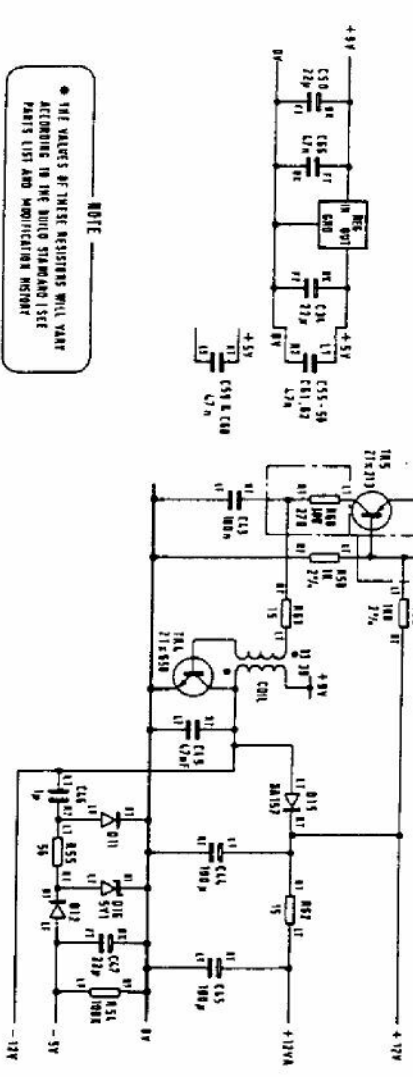


31 - 15.0MA.
 32 - C-33019 MA3 & 10 PPM ABSOLUTE
 ALL OTHERS UNLESS STATED ARE 100%
 ISSUE ON BOARD
 THESE COMPONENTS HAVE BEEN ADDED
 OR CHANGED IN VALUE ON ISSUE
 IN BOARD:
 R60 - WAS 27K, NOW 1K
 C33 - WAS 15PF, NOW 550PF
 C73 - ADDED
 TR1 - ALTERNATIVE TYP231

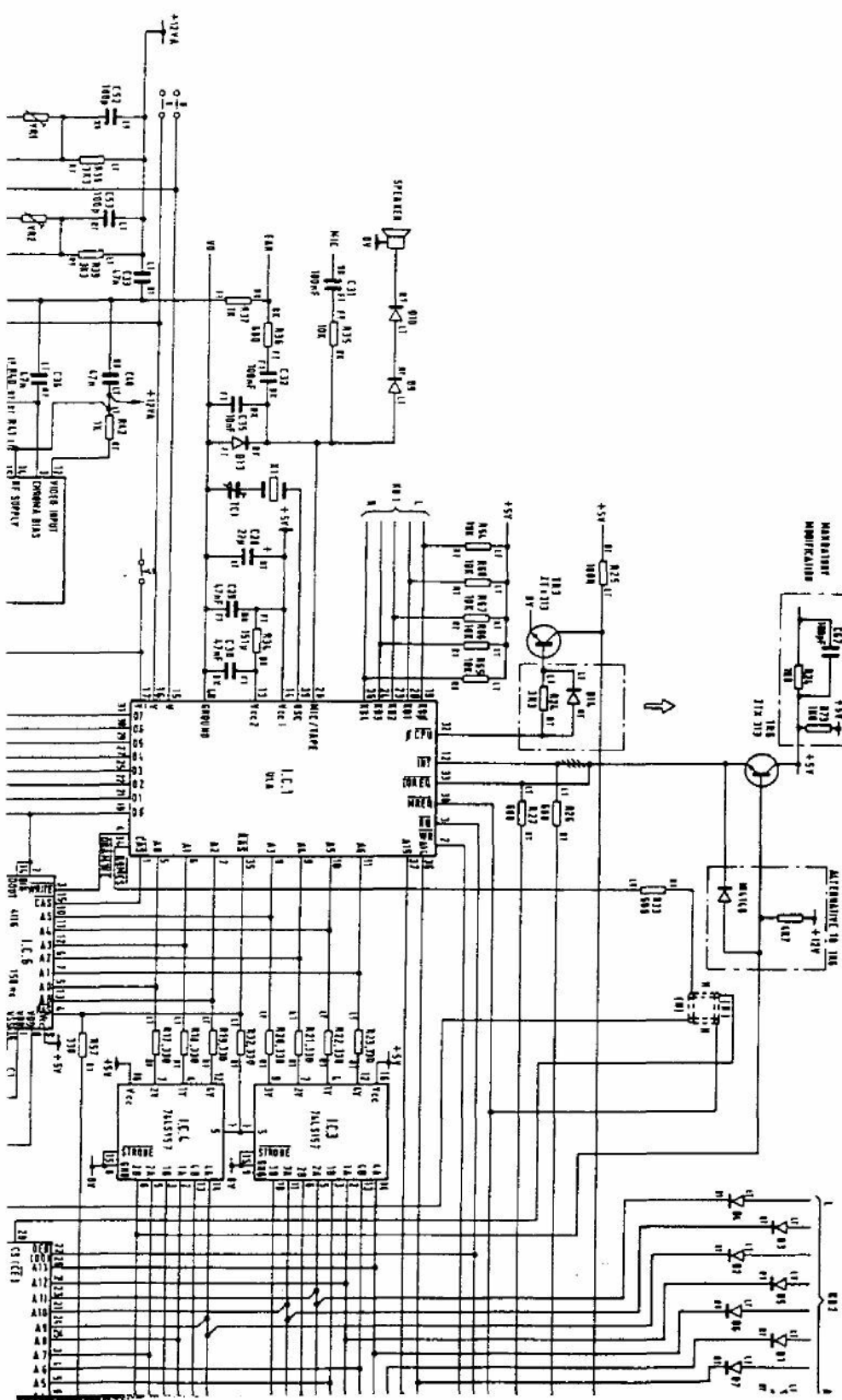
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A3	RES	100K	1/2W
A4	RES	100K	1/2W
A5	RES	100K	1/2W
A6	RES	100K	1/2W
A7	RES	100K	1/2W
A8	RES	100K	1/2W
A9	RES	100K	1/2W
A10	RES	100K	1/2W
A11	RES	100K	1/2W
A12	RES	100K	1/2W
A13	RES	100K	1/2W
A14	RES	100K	1/2W
A15	RES	100K	1/2W
A16	RES	100K	1/2W
A17	RES	100K	1/2W
A18	RES	100K	1/2W
A19	RES	100K	1/2W
A20	RES	100K	1/2W
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A22	RES	100K	1/2W
A23	RES	100K	1/2W
A24	RES	100K	1/2W
A25	RES	100K	1/2W
A26	RES	100K	1/2W
A27	RES	100K	1/2W
A28	RES	100K	1/2W
A29	RES	100K	1/2W
A30	RES	100K	1/2W
A31	RES	100K	1/2W
A32	RES	100K	1/2W
A33	RES	100K	1/2W
A34	RES	100K	1/2W
A35	RES	100K	1/2W
A36	RES	100K	1/2W
A37	RES	100K	1/2W
A38	RES	100K	1/2W
A39	RES	100K	1/2W
A40	RES	100K	1/2W
A41	RES	100K	1/2W
A42	RES	100K	1/2W
A43	RES	100K	1/2W
A44	RES	100K	1/2W
A45	RES	100K	1/2W
A46	RES	100K	1/2W
A47	RES	100K	1/2W
A48	RES	100K	1/2W
A49	RES	100K	1/2W
A50	RES	100K	1/2W
A51	RES	100K	1/2W
A52	RES	100K	1/2W
A53	RES	100K	1/2W
A54	RES	100K	1/2W
A55	RES	100K	1/2W
A56	RES	100K	1/2W
A57	RES	100K	1/2W
A58	RES	100K	1/2W
A59	RES	100K	1/2W
A60	RES	100K	1/2W
A61	RES	100K	1/2W
A62	RES	100K	1/2W
A63	RES	100K	1/2W
A64	RES	100K	1/2W
A65	RES	100K	1/2W
A66	RES	100K	1/2W
A67	RES	100K	1/2W
A68	RES	100K	1/2W
A69	RES	100K	1/2W
A70	RES	100K	1/2W
A71	RES	100K	1/2W
A72	RES	100K	1/2W
A73	RES	100K	1/2W
A74	RES	100K	1/2W
A75	RES	100K	1/2W
A76	RES	100K	1/2W
A77	RES	100K	1/2W
A78	RES	100K	1/2W
A79	RES	100K	1/2W
A80	RES	100K	1/2W
A81	RES	100K	1/2W
A82	RES	100K	1/2W
A83	RES	100K	1/2W
A84	RES	100K	1/2W
A85	RES	100K	1/2W
A86	RES	100K	1/2W
A87	RES	100K	1/2W
A88	RES	100K	1/2W
A89	RES	100K	1/2W
A90	RES	100K	1/2W
A91	RES	100K	1/2W
A92	RES	100K	1/2W
A93	RES	100K	1/2W
A94	RES	100K	1/2W
A95	RES	100K	1/2W
A96	RES	100K	1/2W
A97	RES	100K	1/2W
A98	RES	100K	1/2W
A99	RES	100K	1/2W
A100	RES	100K	1/2W



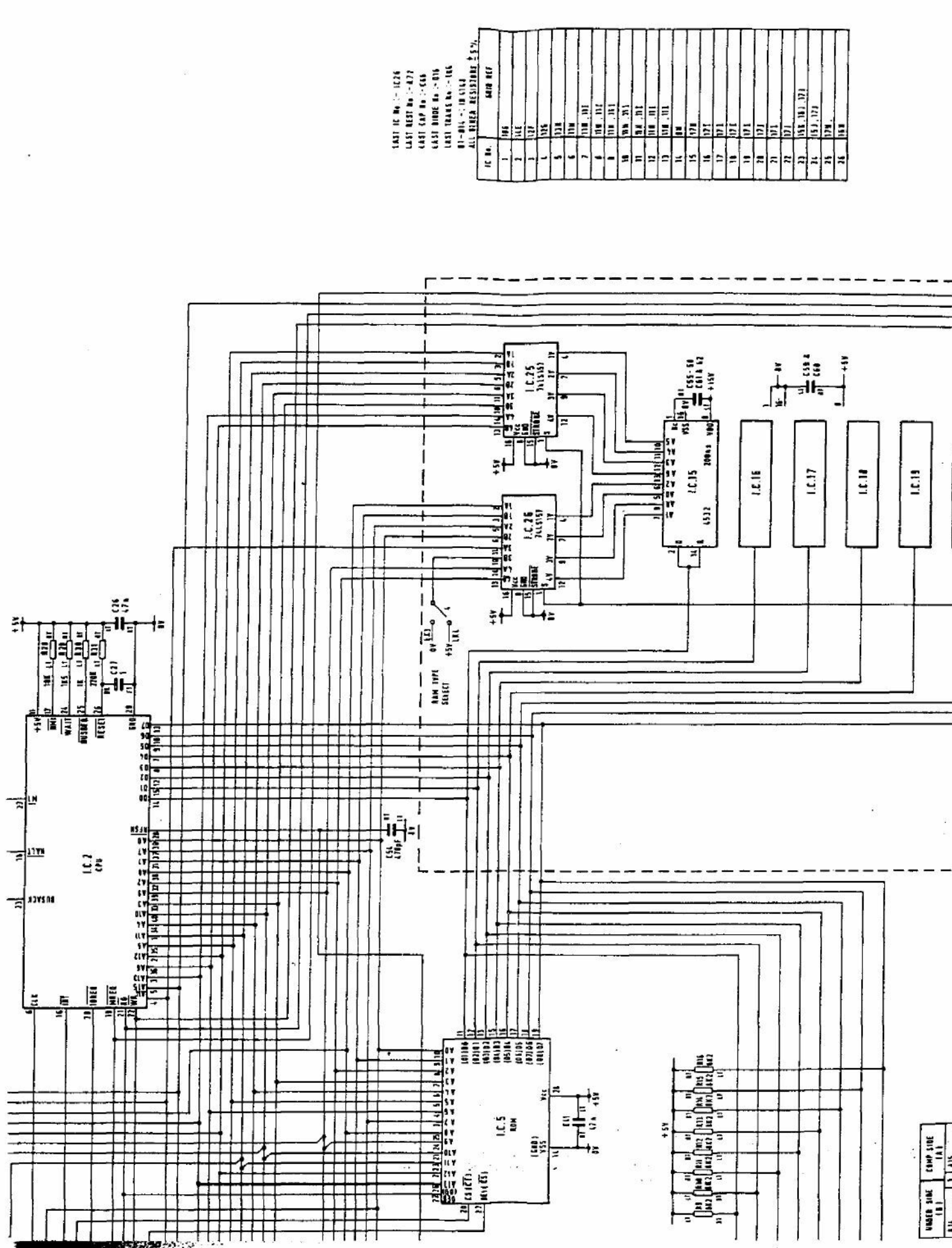
NOTE
 * THE VALUES OF THESE RESISTORS WILL VARY
 ACCORDING TO THE BUILD STANDARD (SEE
 PARTS LIST AND MODIFICATION INSTRUCTIONS)



WIRE SIDE	COMP SIDE
(L.A.)	(L.B.)
A1	1
A2	2
A3	3
A4	4
A5	5
A6	6
A7	7
A8	8
A9	9
A10	10
A11	11
A12	12
A13	13
A14	14
A15	15
A16	16
A17	17
A18	18
A19	19
A20	20
A21	21
A22	22
A23	23
A24	24
A25	25
A26	26
A27	27
A28	28
A29	29
A30	30
A31	31
A32	32
A33	33
A34	34
A35	35
A36	36
A37	37
A38	38
A39	39
A40	40
A41	41
A42	42
A43	43
A44	44
A45	45
A46	46
A47	47
A48	48
A49	49
A50	50
A51	51
A52	52
A53	53
A54	54
A55	55
A56	56
A57	57
A58	58
A59	59
A60	60
A61	61
A62	62
A63	63
A64	64
A65	65
A66	66
A67	67
A68	68
A69	69
A70	70
A71	71
A72	72
A73	73
A74	74
A75	75
A76	76
A77	77
A78	78
A79	79
A80	80
A81	81
A82	82
A83	83
A84	84
A85	85
A86	86
A87	87
A88	88
A89	89
A90	90
A91	91
A92	92
A93	93
A94	94
A95	95
A96	96
A97	97
A98	98
A99	99
A100	100



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
---	---	---	---	---	---	---	---	---	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	-----

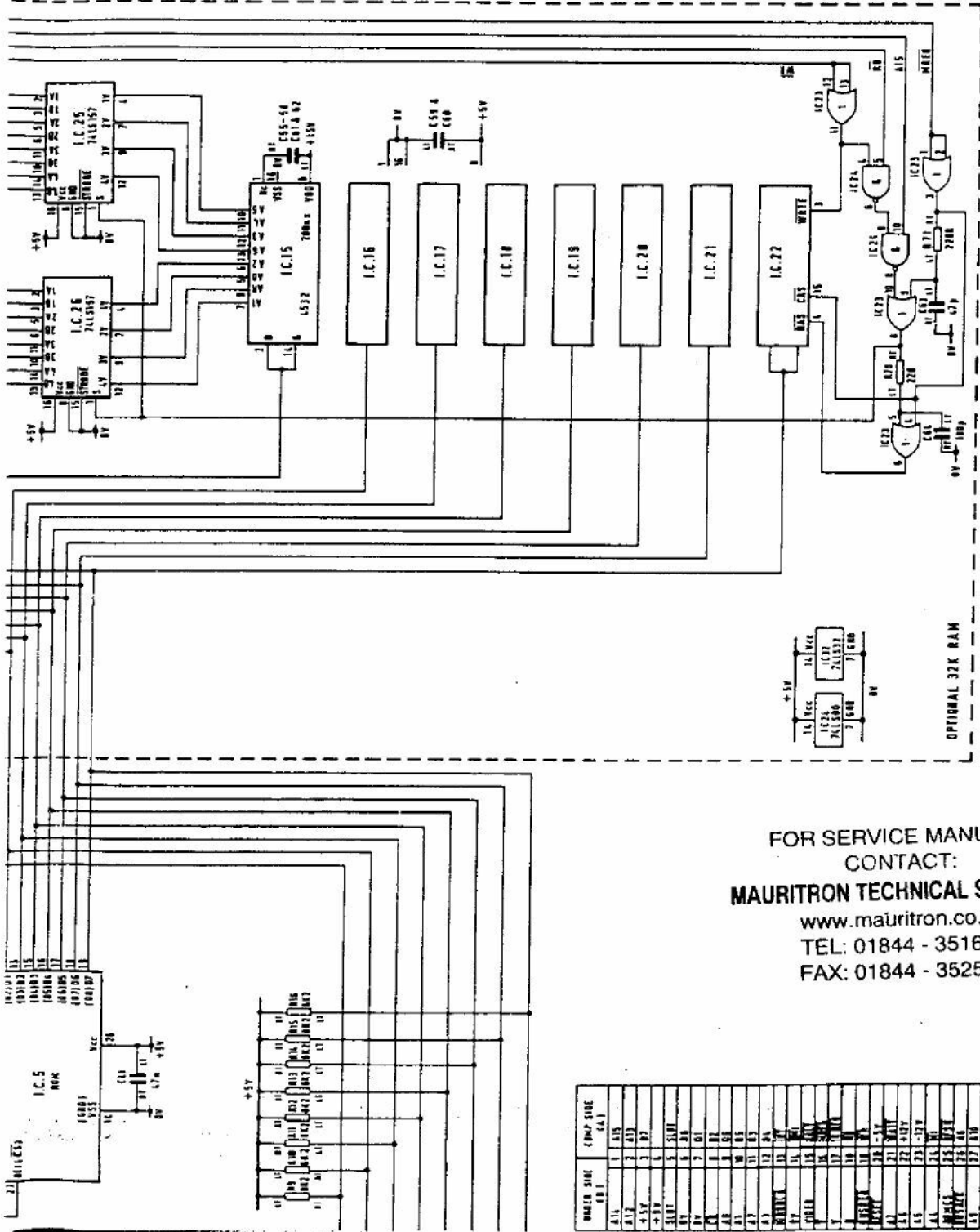


LAST IC NO. = 1026
 LAST REV. NO. = 477
 LAST CAP. NO. = 605
 LAST BIRD NO. = 816
 LAST TRANS. NO. = 185
 BT-816-10-0142
 ALL WIRE RESISTANCE 2.5%
 6408 REV

IC NO.	IC NO.
1	106
2	116
3	127
4	138
5	148
6	158
7	168
8	178
9	188
10	198
11	208
12	218
13	228
14	238
15	248
16	258
17	268
18	278
19	288
20	298
21	308
22	318
23	328
24	338
25	348
26	358

NUMBER	TYPE	COMP. NO.
1	1	1
2	1	1

IC No.	5400 REF.
1	74S05
2	74S15
3	74S17
4	74S24
5	74S28
6	74S30
7	74S31
8	74S32
9	74S37
10	74S38
11	74S40
12	74S41
13	74S42
14	74S44
15	74S45
16	74S47
17	74S48
18	74S49
19	74S50
20	74S51
21	74S52
22	74S53
23	74S54
24	74S55
25	74S56
26	74S57



FOR SERVICE MANUALS
CONTACT:
MAURITRON TECHNICAL SERVICES
www.mauritron.co.uk
TEL: 01844 - 351694
FAX: 01844 - 352554

ORDER SIDE (P1)	COMP. SIDE (P2)
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19
20	20
21	21
22	22
23	23
24	24
25	25
26	26
27	27

ZX SPECTRUM (ISSUE 2) FIG. 1.4
CIRCUIT DIAGRAM ESK 12740
ISSUE 1A